High Volume Manufacturing Based on NanoImprint Lithography on Rough and Non-Planar Substrates

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At the EIPBN 2006 in Baltimore we presented a process and nanoimprint lithography tool being capable for high volume manufacturing of micro- and nano-structured devices. The presented tool employs a high throughput 2-step NIL-process with a first step for manufacturing of an intermediate polymer stamp (IPS®) and a second step employing the IPS® in a simultaneous thermal and UV-imprint (STU®) on the final target substrate.

In this contribution we discuss the advantages of this 2-step HVM-process and its application for industrial production of high brightness LEDs utilizing 2-dimensional photonic crystal and quasi crystal patterns for enhancement of light extraction efficiency and directionality. We will also show an example where this process was successfully applied for printing of nm-structures on curved surfaces such as optical lenses.

Epitaxial overgrowth of III/V-semiconductors on carrier substrates is an important step in LED manufacturing but suffers from growth defects like holes, spikes or larger islands of irregularities (fig.1). This has not been considered as a problem unless further lithographic steps have to be applied after the growth process. The mentioned irregularities are particularly disturbing when NIL-based post processes are utilized for generation of sub-wavelength structured photonic crystal patterns on the compound semiconductor's surface (fig.2, left). Being up to several µm in height these irregularities can cause large defects (void areas without nano-pattern), breakage of the substrate, or in the worst-case breakage of the costly stamp (if hard stamps are applied like in conventional NIL processes).

The IPS®/STU® manufacturing process circumvents this since no hard materials touch each other during the entire NIL sequence. The flexibility of the IPS® allows the stamp to adapt to the curvature and roughness of the substrate (fig.3) thereby enabling uniform residual layers on full wafer scale being essential for high quality pattern transfer in post-imprint processes.

Process and tools have been installed for production at several LED manufacturers' fabs around the world.

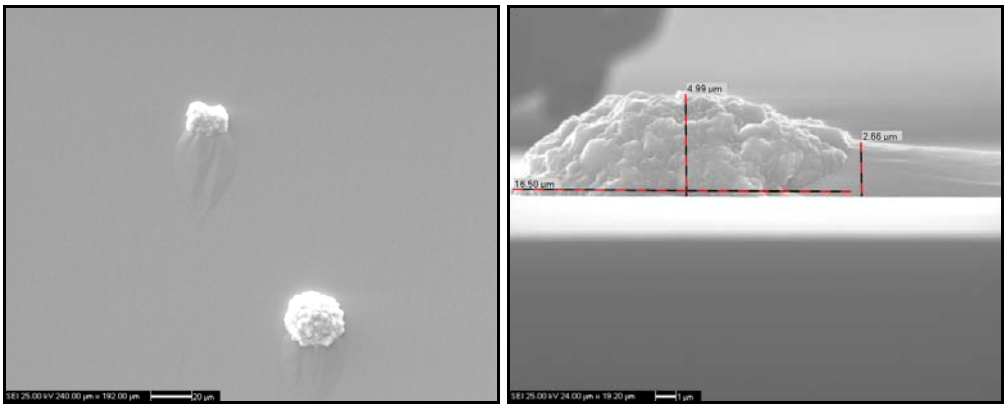

Fig.1: *SEM micrographs showing several µm-sized cauliflower-shaped epitaxial growth defects. It is obvious that imprints with several hundred nm-sized structures in close proximity to these defects are impossible with hard stamps.*

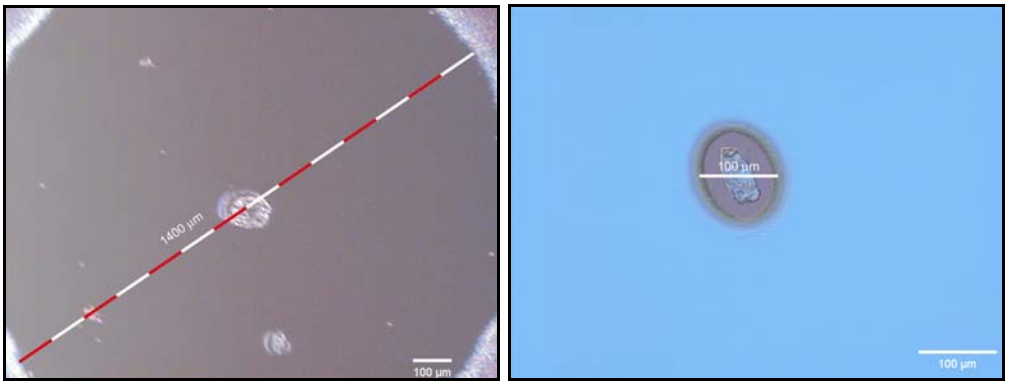

Fig.2: *Optical micrographs showing imprints on GaAs-epi substrates with growth defects of similar size. Left: result obtained with a hard stamp (silicon). Right: Result obtained with an IPS®. The void area on the left is approximately 200 times larger than the void obtained with an IPS®.*

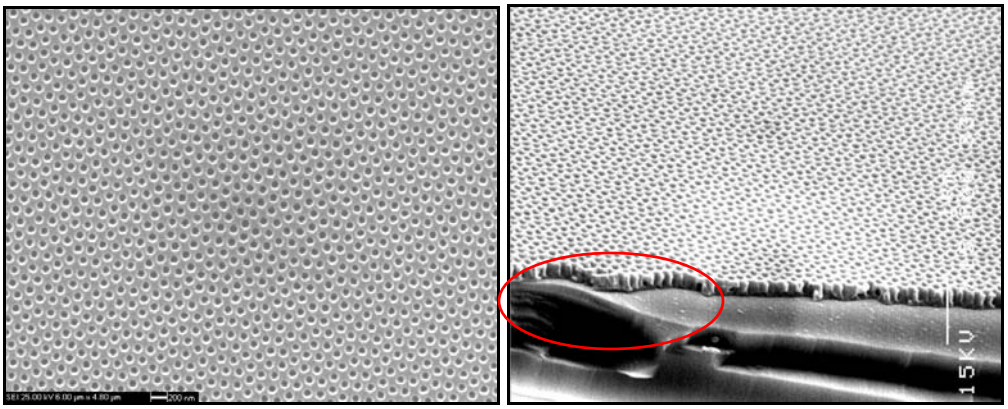

Fig.3: *SEM micrographs of a quasi crystal pattern printed on a GaN epi-layer. The pattern covers the entire surface despite the growth defect shown to the right. The hole diameter is 90 nm.*