Fabrication of Nanoscale Memristor Arrays with One Nanoimprint Lithography Step

Qiangfei Xia*, J. Joshua Yang, Wei Wu, Xuema Li and R. Stanley Williams
HP Labs, 1501 Page Mill Road, Palo Alto, CA 94304

Memristors have wide applications in the next generation non-volatile random access memory and artificial neuron networks, etc [1]. Nanoimprint lithography (NIL) has been demonstrated in making high density cross bar memristor arrays due to its intrinsic advantages [2]. Traditionally, two NIL steps are required in fabrication, one for the bottom electrode and the other for the top. As a result, the critical interfaces in a cross bar junction are inevitably exposed to chemicals and other contaminations, degrading the device performances. Furthermore, fabrication with two NIL steps requires alignments, increases the fabrication cost and lowers the device yield.

To address these issues, here we propose and demonstrate a new fabrication approach for memristors using only one NIL step (Fig. 1). First, cross-shaped trench structures are fabricated in resists by a NIL step and reactive ion etching (RIE). The bottom electrode is angle evaporated into one trench without entering the other one due to the shadow effect. A layer of switching material is then sputter coated on the sample. The top electrode is fabricated using angled evaporation in the other trench, followed by a liftoff process.

In fabrication, a Si substrate with 100 nm thick thermal oxide was cleaned and spin coated with double layer resists. After UV-NIL using a quartz mold with arrays of cross bars, the residual layer in UV-curable resist and the transfer layer were removed using RIE. Evaporation with an oblique angle of 20 degree was then carried out to deposit the bottom electrodes (3 nm Ti/9.5 nm Pt). With this angle, the actual thickness of the metals was calibrated to be 70% of the nominal value. Immediately, a 13 nm thick TiO_x film was sputtered at room temperature, followed by deposition of the top electrodes (12.5 nm Pt) using the 20 degree angled evaporation. The top electrode was finished in two steps by rotating the sample 180 degree to make continuous Pt nanowires. After a liftoff in acetone, the cross bar arrays were finished, with one memristor at each cross point. Figure 2 shows the images of the 1×21 memristor array with 100×100 nm^2 junction areas. Similarly, 21×21 device arrays and devices with junction areas of 40×40 nm^2 were also fabricated.

Figure 3 shows the electrical performance of the devices with 100×100 nm^2 junction areas. The devices can be turned on and off at -3 V and 3 V, respectively and remain the states at zero bias and room temperature, exhibiting non-volatile properties. The ON/OFF ratio at 1V is better than 1000. The switching current is small, suggesting low power consumption of the devices.

With one NIL step for all three layers (two electrodes and a switching layer), the fabrication cost is greatly reduced. This process also introduces fewer defects, less interface contamination, and does not require overlay alignment, improving the device yield and performances. Depositing all layers in-situ enables a real engineering control over the device fabrication, and opens up opportunities to make memories with multiple states per cell.

1. D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, Nature 453, 80-83 (2008).
2. J. J. Yang, M. D. Pickett, X. M. Li, D. A. A. Ohlberg, D. R. Stewart and R. S. Williams, Nature Nanotechnol. 3, 429-433 (2008).

* Email: qiangfei.xia@hp.com; Phone: 650-857-4020.

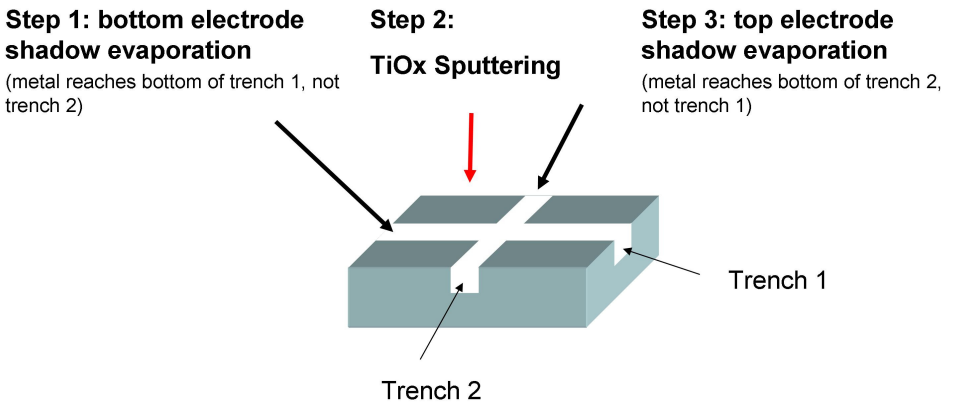

Figure 1. Schematic of our fabrication approach. The cross-shaped trenches are patterned by one NIL step and RIE in resists. After depositing the 3 layers, a liftoff process concludes the fabrication.

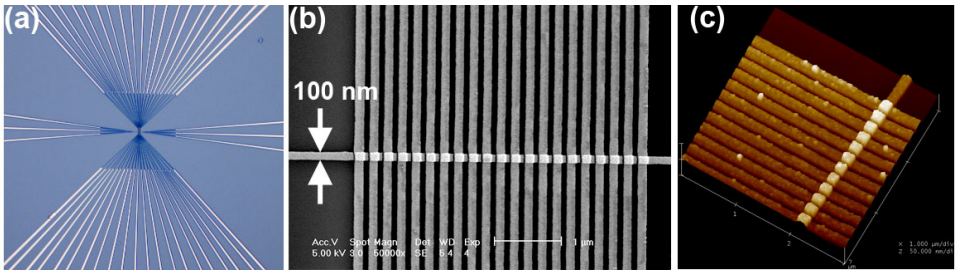

Figure 2. Images of a 1 × 21 array of memristors fabricated using one NIL step. (a) Optical microscope image. (b) SEM image of the junction area. (c) AFM image of part of the array. The junction area is 100 × 100 nm^2.

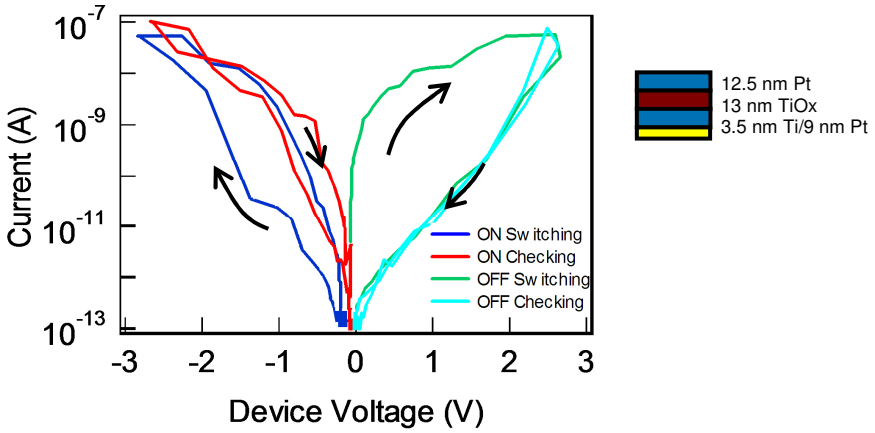

Figure 3. Switching behavior of the memristors fabricated using one NIL step with junction areas of 100 × 100 nm^2. The devices are fabricated on a 100 nm thick thermal oxide capped Si wafer, with 13 nm thick TiO_x sandwiched between the 12.5 nm thick Pt top electrodes and the 9 nm Pt /3 nm Ti bottom electrodes. The devices exhibit non-volatile switching behavior with an ON/OFF ratio larger than 1000 at 1V.