Hydrogen silsesquioxane-based hybrid electron beam and optical lithography for high density CMOS prototyping

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Hybrid lithography is a term broadly applied to describe the use of two or more lithography techniques to create a composite pattern. A variety of methods to combine photolithography and electron beam lithography (EBL) in a single layer of resist have been reported[2-3]. These techniques leverage the flexibility and high resolution patterning capabilities of EBL while capitalizing on the high throughput nature of photolithography to print lower resolution features. While this approach is useful, identifying a process window where both exposures are optimized can be challenging and frequently requires tight coordination of all lithographic processing[2-3].

In this paper we report a hybrid lithography process that decouples the EBL and optical exposures by using a two resist scheme. In brief, substrates are coated with an anti reflective coating (ARC) and a hydrogen silsesquioxane (HSQ)-based EBL resist (XR1541, Dow Corning, Fig 1-a). A pattern is exposed using EBL and developed using a TMAH based N=0.26 developer (Fig 1-b). Photoresist is coated onto the substrate (Fig 1-c) and the optical pattern is exposed and developed (Fig 1-d). In this work, positive and negative tone 248 nm resists were used without modifying the baking or develop cycles practiced in standard photolithography. The ARC layer is opened using the photoresist and HSQ as the etch mask followed by pattern transfer into the substrate with reactive ion etching (RIE, Fig 1 e-f). An example of patterns printed using this approach is shown in figure 1 (g-i).

We have used HSQ-hybrid lithography to explore the scaling of trigated FinFET devices[4] to densities suitable for the 22 node. The process flow for fabricating these devices is outlined in figure 2. Transmission electron microscope (TEM) images of completed devices are shown in figure 3. HSQ-based hybrid lithography was used to pattern the Si active regions and gate electrodes with a minimum pitch of 50 and 90 nm respectively. Electrical results from single devices and a CMOS inverter are shown in figure 4. To the best of our knowledge this is the first demonstration of trigated FinFET CMOS circuitry with a contacted gate pitch below 110 nm[5].

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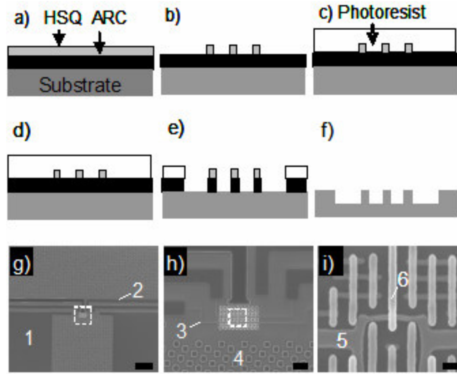

Fig 1: (a-f) HSQ-based hybrid lithography process. (g) Scanning electron microscope (SEM) images showing an example of a two level pattern printed using this technique showing (1) probing pads and (2) coarse interconnects printed by photolithography. The region of interest (ROI) highlighted in (g) is shown in (h) displaying (3) interconnects printed by EBL and (4) fill features printed by photolithography. The ROI in (h) is shown in (i) displaying (5) active area and (6) gate level features patterned with EBL. The scale bars in (g – i) are 10, 2 and 0.1 μm, respectively.

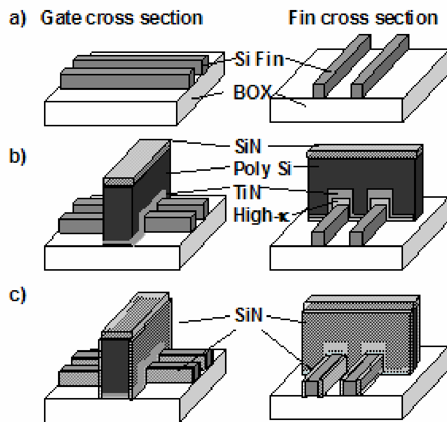

Fig 2: The devices fabricated for this work were built on Si on insulator wafers with a 30 nm-thick Si layer and a 140 nm buried oxide (BOX) layer. HSQ-based hybrid lithography and RIE were used to define active Si regions, referred to as fins (a). A gate stack consisting of an Hf-based high-κ gate dielectric, a TiN gate electrode, a poly-Si film and a SiN capping layer was deposited and patterned using HSQ-based hybrid lithography and RIE (b). A ~6-7 nm SiN offset spacer was formed through deposition and RIE (c). EBL was used to define implant blocking patterns for NMOS and PMOS devices and extension implants using As^+ and B^+ species were performed respectively. A thin Ni silicide was formed and the devices were contacted using W vias and wiring.

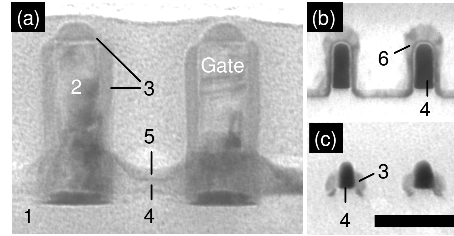

Fig 3: TEM images of a completed device. (a) Gate cross section obtained from devices with a 90 nm gate pitch. (1) BOX (2) Poly-Si (3) SiN (4) SOI fin (5) NiSi. The gate wraps around the fin causing a projection of both in the channel regions. The gate length is ~22 nm (b) Cross section through the fins in the gate stack region showing (6) TiN and high-κ gate dielectric. (c) Cross section through the fins in the source/drain region. All images are shown at the same scale. The scale bar shown in (c) is 50 nm.

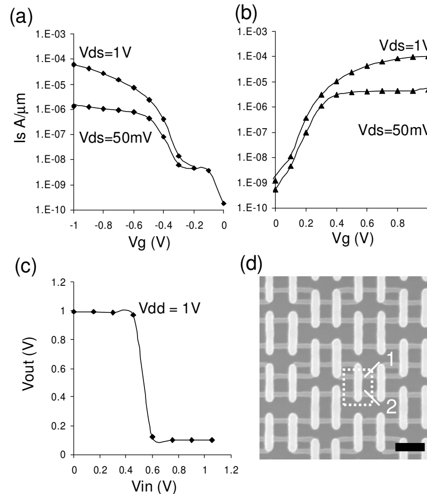

Fig 4: Source current, Is, vs. gate voltage, Vg, at a 1 V and 50 mV drain-to-source bias, Vds, from (a) PMOS and (b) NMOS devices working at a 90 nm gate pitch. The width-to-length ratio of both transistors is 70/22 nm. (c) Transfer curves from a CMOS inverter circuit with a 90 nm gate pitch and a minimum fin pitch of 50 nm operated at 1 V. (d) SEM image showing the layout of (1) PMOS and (2) NMOS devices arranged in a 6-transistor static random access memory array configuration. A single inverter is outlined. The density of these inverters is compatible with a bit cell area of 0.045 μm^2. The scale bar is 100 nm.