Locally-Gated, Suspended Silicon Nanowire FETs for Biomolecular Sensing

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We present a wafer-scale process for fabricating individually-gated suspended nanowire sensors on SOI. Globally-backgated nanowires were used previously for label-free immunodetection [1]. Local gate control enables inversion and accumulation mode devices on the same chip allowing complementary circuits for differential sensing. In addition, local gating allows individual trimming of each device on a chip to maximize sensitivity. Suspended wires have greater surface area exposed for sensing and may also avoid some of the sensitivity limitations inherent to surface bound nanowires sensors in laminar flow [2]. Additionally, the suspended nanowire devices may exhibit interesting nano-electro-mechanical properties.

The key steps in the fabrication process are outlined in Figure 1. Prior to patterning, a gate dielectric and polysilicon gate layer are deposited on an ultra-thin-active SOI wafer. The source and drain contact pads and nanowire channels are patterned by electron beam lithography (EBL) in hydrogen silsequioxane (HSQ). This pattern is subsequently transferred into the gate stack by reactive ion etching (RIE). Channel widths ranging from 2um to 20nm are achieved. A gate region is then defined by UV lithography or EBL and an RIE step simultaneously removes the polysilicon gate and gate dielectric from the contacts while etching the active silicon from the area surrounding the devices. A low energy ion-implantation dopes the source and drain regions while the channel remains protected by the resist that was used to pattern the gate. The resulting structure is covered with a PECVD or spin-on dielectric and a window is opened over the device channel, after which the channel is defined by an anisotropic wet etch using tetramethylammonium hydroxide. This results in a nanowire channel with smooth, well defined facets. Vias are etched to contact the source drain and gate and the contacts are metalized. Finally, the devices are coated with SU-8 and the nanowire channels of the devices are undercut using hydrofluoric acid.

Using unreleased locally gated devices we demonstrate very favorable transistor characteristics as compared to previously fabricated backgate-only devices. Subthreshold slope as low as 75mV/decade is observed with an on to off current ratio greater than $2x10^6$. Field-effect mobilities of 1200 cm^2/V-s for electrons and 400 cm^2/V-s for holes are reported.

The nanowire devices described here will be useful for a variety of bio-molecular and immunological sensing experiments and preliminary sensing measurements using these devices will be presented.

1. E. Stern et al, Nature, **445**, 519 (2007).
2. P. E. Sheehan and L. J. Whitman, Nano Lett., **5**, 803 (2005).

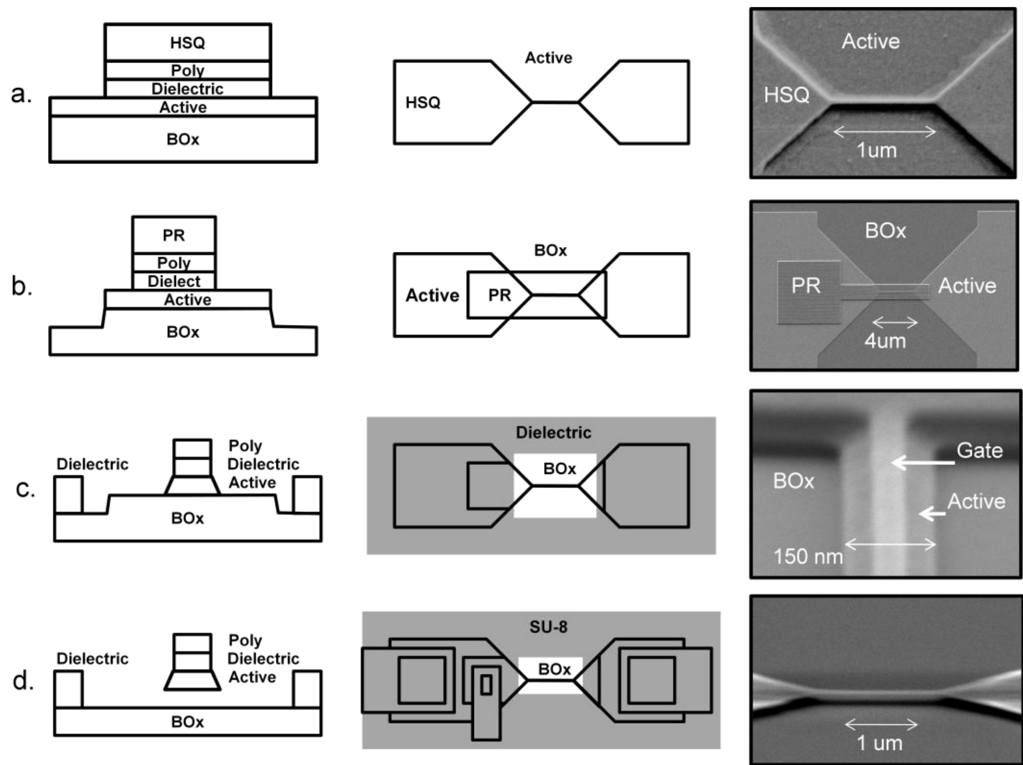

Figure 1: Process for fabricating nanowire sensor devices. (a.) Gate dielectric and polysilicon gate layer are deposited on SOI wafer. Contact pads and channel are patterned with HSQ using EBL and gate stack is etched with RIE. (b.) Gate region is patterned with EBL or UV lithography and pattern is transferred by RIE into remaining gate stack. Active layer surrounding contact pads is simultaneously etched. Source and drain regions are doped by ion implantation. (c.) PECVD or spin-on dielectric is deposited and patterned to open window over nanowire channel. Gate pattern is transferred into active silicon by anisotropic wet etch to form device channel. <111> facets of channel are clearly visible in micrograph. (d) Vias are etched and contacts are metalized. Surface of wafer is passivated with SU-8 except for window over device channel. Finally devices are undercut using hydrofluoric acid.

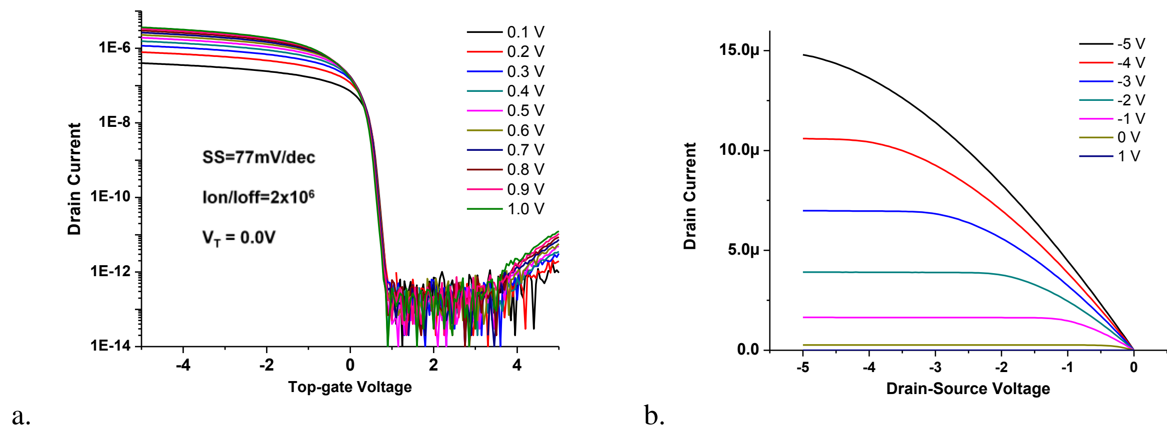

Figure 2: Field effect transistor characteristics of accumulation-mode nanowire device. (a.) Drain current versus source-drain voltage at various gate voltages. (b.) Drain current versus gate voltage at various source-drain voltages.