Fabrication of poly(3 -hexylthiophene) (P3HT) in-plane gate transistors by low temperature thermal nanoimprint lithography

J. Kettle[1], S. Whitelegg[1], Y.M. Sun[1], Y.Luo[1], A.Song[1], M.B. Madec[2], M.L. Turner[2]
1 Microelectronics and nanostructures group, School of Electrical and Electronics engineering, University of Manchester, Sackville St., Manchester, M60 1QD, UK
2 Organic Materials Innovation centre (OMIC), School of Chemistry, University of Manchester, Oxford road, Manchester, M13 9PL, UK

OFETs based on solution-processible polymeric and small molecular semiconductors have obtained impressive improvements in performance with mobility of up to 1.8$cm^2V^{-1}s^{-1}$ being demonstrated [1]. Generally, fabrication occurs with 3D-OFET structures; the most commonly used geometry is bottom gate with top contacts. Recent work by Song *et al.* has developed a novel 2-D device; a self switching diode (SSD) fabricated from AFM lithography [2]. Using this approach, the organic SSD was fabricated with the output voltage operational at 30MHz [2]. To further improve the functionality of Song's work, the SSD can be remodelled to include a side-gate perpendicular to the device's channel in order to control the flow of current through the channel; a device commonly referred to an in-plane gate (IPG) transistor. IPG transistors can realise control of the electric field parallel to the two-dimensional electron gas (2-DEG), which results in a strong potential confinement in the 1-D channel. IPG transistors were first introduced in AlGaAs/GaAs two-dimensional electron gas (2DEG) by Wieck *et al.* [3]. In this paper, we further previous work by proving that IPG transistors can be fabricated into poly(3 -hexylthiophene) (P3HT). We have developed a new approach to pattern organic semiconductors at the nanoscale; this involves NIL processing using poly-butylmethacrylate (PBMA) as a mask layer and argon milling to remove the residual and also to create isolating lines in the P3HT film. PBMA was preferred over conventional NIL polymers such as PMMA, as processing was achievable at low temperatures.

When measuring the electrical performance of the left-gate of the devices shown in fig. 1, the transfer curve of the device shows the on-off ratio (I_{ON}/I_{OFF}) was measured at $3.82x10^2$ and threshold Voltage (V_{TH}) was measured at 31.3V. Due to the choice in substrate used in this work (n++ Silicon with 300nm SiO_2 top surface acting as a dielectric), the device can also operate as a wire transistor. Overlaid on the side-gate transfer characteristics in fig. 2 is the back-gate performance of the device. We observe, V_{TH}=18.55V and $I_{ON}/I_{OFF} = 6.14x10^3$. Reasons for this discrepancy between back and side gate are discussed in this paper. Furthermore, we demonstrate that limitations of the air stability if P3HT can be overcome by incorporating a PMMA buffer layer, which inhibits oxygen and water degradation. This enables the device to exhibit a decrease of only 30% of the initial value over a 15 day period; this decrease is minor compared to the rapid degradation experienced by conventional P3HT devices in ambient air. Finally, we demonstrate the suitability of P3HT-based IPG transistors as highly sensitive chemical detection sensors.

[1] J. E. Anthony, *Angew. Chem. Int. Ed.* 47, 452 – 483 (2008)
[2] A. M. Song *et al. Nano Letters*, Vol. 5, No.7, pp. 1423 (2005).
[3] A. D. Wieck *et al. Appl. Phys. Lett.* 61, 1048 (1992),

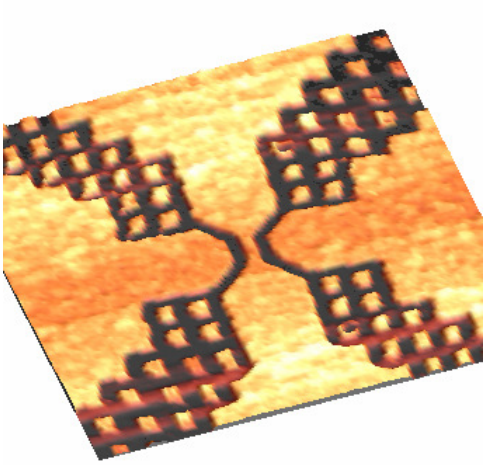

Figure 1: AFM micrograph of the poly(3 -hexylthiophene) (P3HT) IPG-transistor showing bottom contact (source) and the top contact (drain). Control of the flow of current through the channel is achieving by biasing either left or right terminal, or alternatively via the back gate (as the substrate is n++ Silicon with 300nm SiO_2 top surface acting as a dielectric).

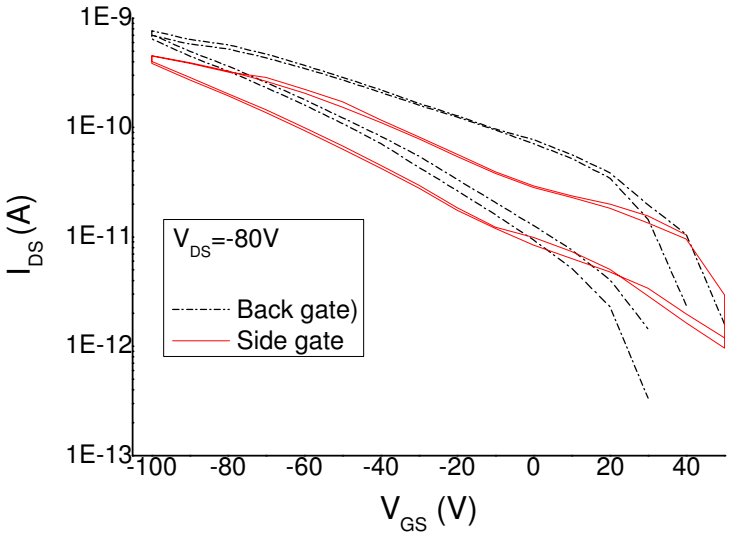

Figure 2: FET transfer characteristics of a poly(3 -hexylthiophene) (P3HT) IPG-transistor at room temperature showing (dashed line) side-gated performance and (solid line) showing the back gate performance. The applied drain-source Voltage, V_{DS} in both instances was -80V.