Reconfigurable Logic Circuits in a Memristor-Transistor Hybrid Chip

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The IC industry has been following the Moore's Law by continually shrinking the feature size of circuit elements using advanced lithography technologies. However, with feature size becomes smaller and smaller, shrinking is not only economically expensive, but also technically challenging. To address this issue, several alternative approaches such as "bottom-up" scheme to chemically synthesize active device components, and CMOS/molecular hybrid circuit architecture [1] were proposed, but few of them is practical to build integrated circuits.

Here we demonstrate a memristor-transistor hybrid circuit where memristors are integrated with CMOS substrate vertically. The memristors serve as the data routing network, connecting the transistors on the CMOS layer to form logic circuits (Fig. 1). This architecture not only results in a smaller chip size and higher processing speed, it can also route defects around, leading to a highly defect-tolerant circuit [2].

To fabricate the hybrid circuits, CMOS substrates from a commercial foundry were first planarized using a UV-curable liquid material. W vias in CMOS were exposed using photo-lithography and reactive ion etching (RIE), followed by deposition of metals pads to the level of the planarized surface and a liftoff process. Nanoimprint lithography (NIL) was carried out to pattern the bottom electrode (9 nm Pt/2 nm Ti). A 36 nm thick TiO_x layer was sputtered on as the switching material. The top electrode (12 nm thick Pt) was fabricated using NIL on the switching layer with contact pads connected to the CMOS layer. The images of the CMOS substrate and the hybrid chip are shown in Fig. 2. At each cross bar junction, the metal/TiOx/metal sandwich structure forms a memristor [3].

In order to pass the information through, the memristors are configured (turned ON or OFF) first using a voltage larger than the operational voltage. Fig. 3 shows a typical configuring I-V curve where a junction is turned on. After the junctions were configured, computation was carried out at a small logic-swing voltage so that the configuration was not changed. Fig. 4 shows an example signal path in the hybrid circuit: the output of gate A goes up through a red via, through a nanowire, through the junction (J) (memristor), through a second nanowire, down through a blue via, to reach the input of gate B.

With several selective memristors turned on, digital circuits were wired up on the hybrid chip. Fig. 5 shows the computing results for the AND, OR, NOT, NAND and NOR gates and a positive edge triggered D flip-flop. With these basic logic gates implemented, the hybrid chip is capable of performing more complicated computations.

In summary, we have demonstrated the first hybrid memristor-transistor integrated circuit with successful implementation of the logic functions. With our current design, the defects in a circuit can be routed around, and the memristors can be re-configured to be open or closed, giving flexibility in circuit design. This hybrid circuitry integrates new materials into Si-based electronics for complex functionalities, suggesting that both memristors and their enabling technology NIL are compatible with a logic-type CMOS process without changing the infrastructure in the current IC industry.

1. D. B. Strukov and K. K. Likharev, Nanotechnology 16, 888-900 (2005).
2. G. S. Snider and R. S. Williams, Nanotechnology 18, 035204 (2007).
3. D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, Nature 453, 80-83 (2008).

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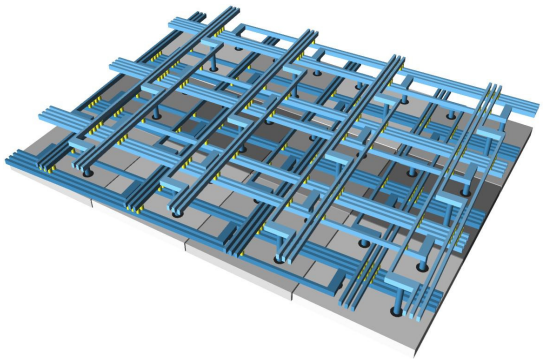


Fig. 1. Schematic of the memristor-transistor hybrid chip in which the memristors are the configurable wiring used for wiring up the transistors to make a digital circuit. The gray substrate is the CMOS layer. The switching material (yellow) and pairs of blue wires form memristors that are connected to the CMOS through the blue pins.

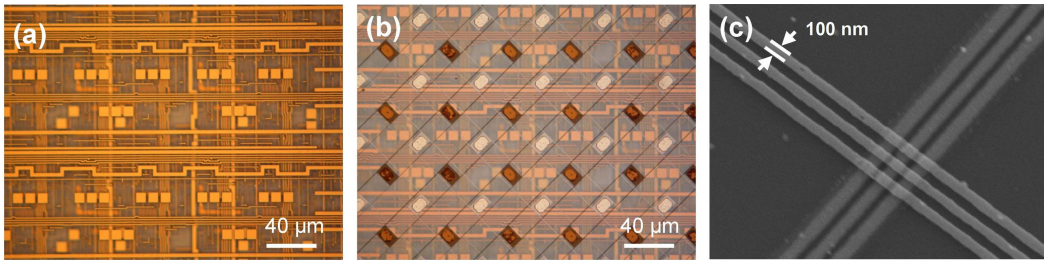


Fig. 2. (a) Optical image of the CMOS chip. (b) CMOS with memristors integrated on top. (c) SEM image of a memristor array with junction arrays of 100 × 100 nm^2.

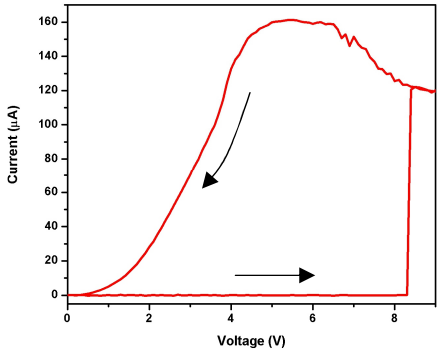


Fig. 3. An I-V curve during the configuration of a memristor, which is turned on at 8.3V in this case.

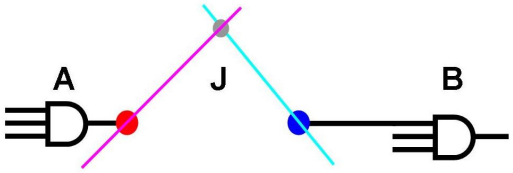
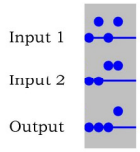


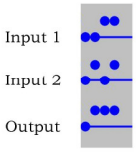
Fig. 4. Schematic of a signal path in a logic circuit. A and B are transistors and J is the memristor.

AND gate



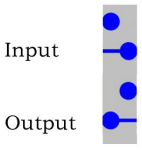
	VOLTAGES (V)			
$V_{input\ 1}$	-0.001	3.299	-0.001	3.299
$V_{input\ 2}$	-0.001	-0.001	3.297	3.298
V_{output}	-0.004	-0.005	-0.005	3.295

OR gate



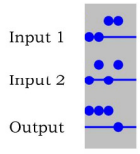
	VOLTAGES (V)			
$V_{input\ 1}$	0.002	0.000	3.297	3.298
$V_{input\ 2}$	0.000	3.297	-0.000	3.297
V_{output}	-0.004	3.297	3.297	3.296

NOT gate



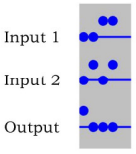
	VOLTAGES (V)	
V_{input}	3.300	0.002
V_{output}	-0.001	3.296

NAND gate



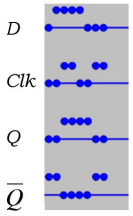
	VOLTAGES (V)			
$V_{input\ 1}$	-0.000	0.002	3.300	3.300
$V_{input\ 2}$	0.002	3.300	0.001	3.300
V_{output}	3.298	3.301	3.298	0.001

NOR gate



	VOLTAGES (V)			
$V_{input\ 1}$	-0.002	-0.001	3.296	3.292
$V_{input\ 2}$	0.000	3.294	-0.001	3.297
V_{output}	3.291	-0.005	0.003	-0.007

D Flip-flop



	VOLTAGES (V)	
D	3.300	0.000
Clock	Rising	Rising
Q	3.300	0.000
$\overline{Q}$	0.000	3.300

Fig. 5. Configured logic cicuits in the memristor-transistor hybrid chip. In each case, the lower blue dots are logic "0"s and the higher ones are logic "1"s. The measured truth tables are listed with the visualization results.