# Sidewall spacer double patterning technique with reduced process complexity

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Double patterning (DP) has emerged as the most promising candidate for imaging at the 32nm node. A variety of double patterning techniques exist including litho-etch-litho-etch (LELE), litho-freeze-litho-etch (LFLE), sidewall spacer, etc. In this study, a process scheme utilizing a resist freeze process to significantly simplify the sidewall spacer DP is explored. Upon vapor phase reaction (VPR) in a track compatible reaction chamber, the freeze material cross-links with both the sidewall and the top portion of the exposed pattern. The thickness of the reacted portion of the pattern is dependent on the freeze material, flow rate, bake temperature and time. A subsequent oxygen reactive ion etch ($O_2$ RIE) step will first remove the top portion of the photoresist, leaving the un-reacted photoresist exposed by the excessive photons inside the RIE chamber. After removing the exposed photoresist, the crosslinked sidewall could then act as an etch mask for pattern transfer. The process is simplified over more common sidewall spacer approaches by replacing the CVD-CMP-etch-stripping process with a three-step VPR-RIE-development process. Repeating the process with an interdigitating mask allows for patterns between two groups of spacers, leading to higher harmonic patterning.

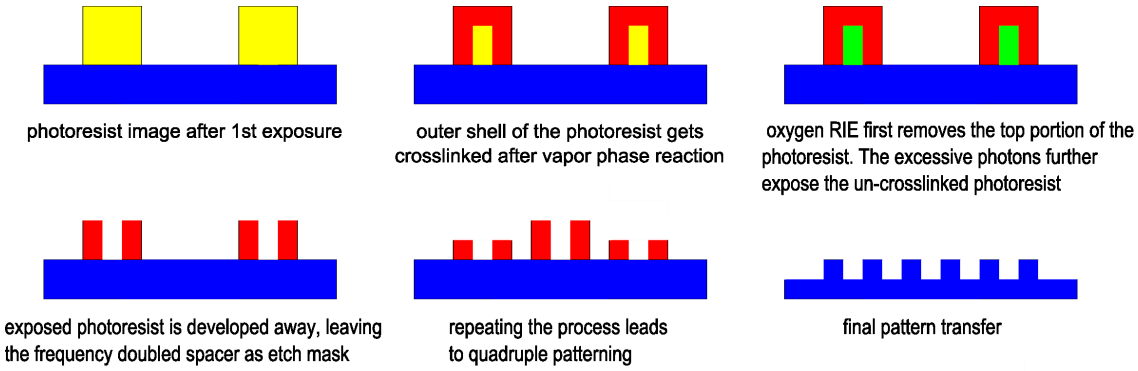


*Fig 1:* The process flow of the proposed sidewall spacer double patterning technique