

Pattern placement error due to resist charging effect at 50kV e-beam writer

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As semiconductor features shrink in size and pitch, the pattern placement error at photomask has been interested as an important factor to be reduced. Especially, the development of double exposure technique for sub-45 nm node requires the pattern placement error to be less than 4 nm. Among various sources of pattern placement errors, here, we focus on the error occurring from resist charging effect.

In e-beam lithography, electron exposure results in charging of the insulating resist. The deposited charge in resist layer generates electric field and it deflects the path of electron beam [1,2]. Many previous studies have reported the effect of resist charging on the pattern displacement error but they have focused on the charging effect in low energy e-beam lithography. Although a few papers have reported recently the resist charging effect in 50kV e-beam lithography, they also have the limitation when understanding the charging effect in photomask for mass production.

Here, we present the charging effect in FEP-171 resist at e-beam writer with accelerating voltage of 50kV and its effect on pattern placement error of photomask, as shown in Fig. 1. Based on simulation and experiment, we propose the model to describe resist charging effect in photomask and the pattern placement error. Our model is based on the electric force calculation between the injected e-beam and the charges in resist that are generated by primary electrons and scattered electrons. Furthermore, we present the pattern qualities such as line edge roughness and uniformity of pattern size also can be affected by resist charging effect.

¹ M. Bai, D. Pickard, C. Tanasa, M. McCord, C. Berglund, and R. Fabian W. Pease, Proc. SPIE 3546, 383 (1998)

² N. Nakayamada, S. Wake, T. Kamikubo, H. Sunaoshi, and S. Tamamushi, et. al.,
Proc. SPIE 7028, 70280C (2008)

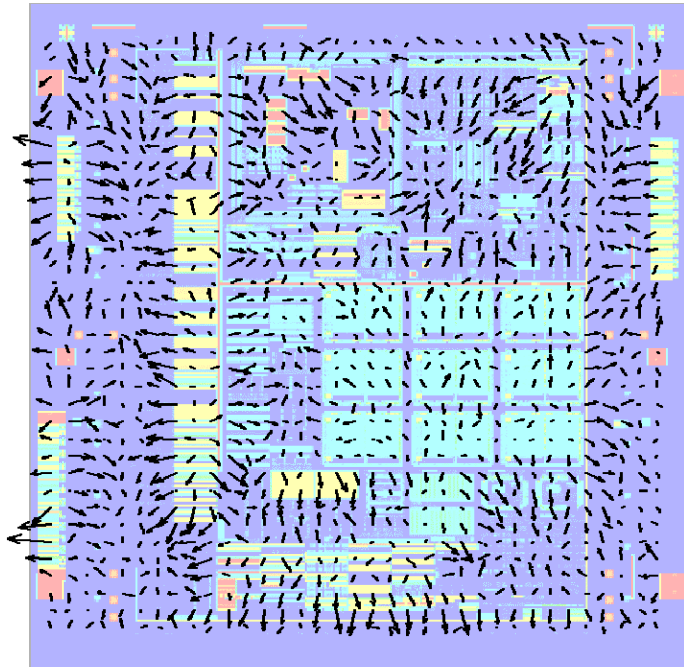


Fig. 1: Pattern placement error due to resist charging effect in photomask