Wafer Topography Proximity Effect Modeling and Correction for Patterning the Implant Layer

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Photolithography on reflective surfaces with topography can cause additional exposure in some areas in the photo resist, resulting in undesired critical dimension (CD) variations in the printed patterns. Using bottom anti-reflective coatings (BARCs) will reduce the severity of the problem. However that's not a preferred solution in some situations due to added process complexity. This is the case for implant layer patterning.

This topography proximity effect (TPE) in implant layer patterning has been ignored in the mask synthesis flow for the 45nm and larger nodes due to its relatively small impact to the CDs and the implant layer is one of the so-called noncritical layers. When the device critical length reaches 32nm and lower, the variations on the implant layer caused by underlying topography becomes more and more an issue and need to be addressed in the mask synthesis flow. In order to do that, simulation with non-planar stack is required. The available tools for photolithography simulation with wafer topography, such as Synopsys' Sentaurus Lithography, adopt a rigorous approach based on the Maxwell equations, and hence unfit for full chip optical proximity correction (OPC) due to their long runtimes. A fast method for TPE simulation is needed to make wafer topography proximity correction (TPC) feasible.

In this paper, we propose an approximate method that captures TPE reasonably well, and it fits in the current OPC flows easily. We validate the method's accuracy by comparing its simulation results with those produced by Sentaurus Lithography. We also show how it helps implant layer mask synthesis that takes TPE from previous layers, such as the shallow trench isolation (STI) and gate layers, into consideration.