Design specific variation in via/contact pattern transfer - Full chip analysis

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Optimization of the semiconductor processing steps involved in the pattern transfer is a challenge which becomes more and more critical with the further scale reduction. While the existing simulation capabilities of predicting the post-illuminated and post-photo resist development contours are in line with the current requirements, the prediction of the post-etch contours is less robust.

Via-contact etch process step is traditionally considered to be one of the most technically challenging step in semiconductor processing. Determination of the process window, which covers all issues associated with the pattern density variations, remains to be a serious problem. The cause of this problem is in well-known phenomenon of microloading, which is an across-layout steady state variation in concentration of neutral radical species participating in etch related surface reactions. Traditionally via/contact etch process optimization is done for regular patterns on test wafer. Employed patterns represent a small part of the entire test-chip design. Etch rate variation caused by microloading is governed by a large-scale pattern density variation, of order of magnitude of the mean free path of radical species participating in etch reactions, which is much larger than the size of used patters. Full-chip analysis is required for understanding the pattern dependency of the etch step.

We have developed a novel model-based full-chip algorithm providing a capability to control the design specific variation in pattern transfer caused by via/contact etch processes (VCE). Physical model for the etch rate of an arbitrary feature, incorporated into the developed algorithm, takes into account both the phenomena: an across-die variation in neutral species fluxes caused by the global pattern density variation (microloading) and aspect ratio-induced variation in intra-feature radical transport resistance. Because there is a 6-7 orders-of-magnitude difference between the wafer size and a layout feature size, a die-level model is necessary as it provides a link between wafer-level and feature-level simulation tools, and models layout-induced intra-die etch rate variation. Coupling to a lithography model provides a capability to control pattern transfer into the contact stack during the etch process. A realistic set of process parameters employed by the developed model allows using VCE for the design aware process optimization in addition to the “standard” process aware design optimization. All the information about the die layout is implicit in the solution, so there is no need for the analyzed etch step to be run on a specially designed test chip. VCE model was successfully validated and calibrated on real silicon for a variety of etch steps employed by a number of chip manufacturers.

As an example of VCE application we demonstrate a detection of etch-induced hot spots in a particular design. By introducing the treshold etch rates as conditions for via under- and over-etch we can program the software to find locations of all suspicious vias which can result a catastrophic failure. VCE can predict via/contact bottom CD variation for every step of a multistep etch receipe and report the etch hotspots based on the fab defined thresholds of acceptable variations in a prospective etch step. Different correction scenarios that should be undertaken either from design side or manufacturing can be evaluated with this tool. Smart dummy insertion based on the VCE analysis or adjustment of a drawn in GDSII CD size for specific via/contact locations determined by VCE at the MDP stage are examples of the design related correction. Another possible way is the design-specific optimization of process parameters by employing VCE linked with the robust reactor-scale model. Slight modification in the plasma gas-phase composition caused by process paramets adjustment, calculated in the reactor-scale model, provides VCE with the modified values of internal code parameters, which generate a modified radical flux distribution and result in changes in CD variation.

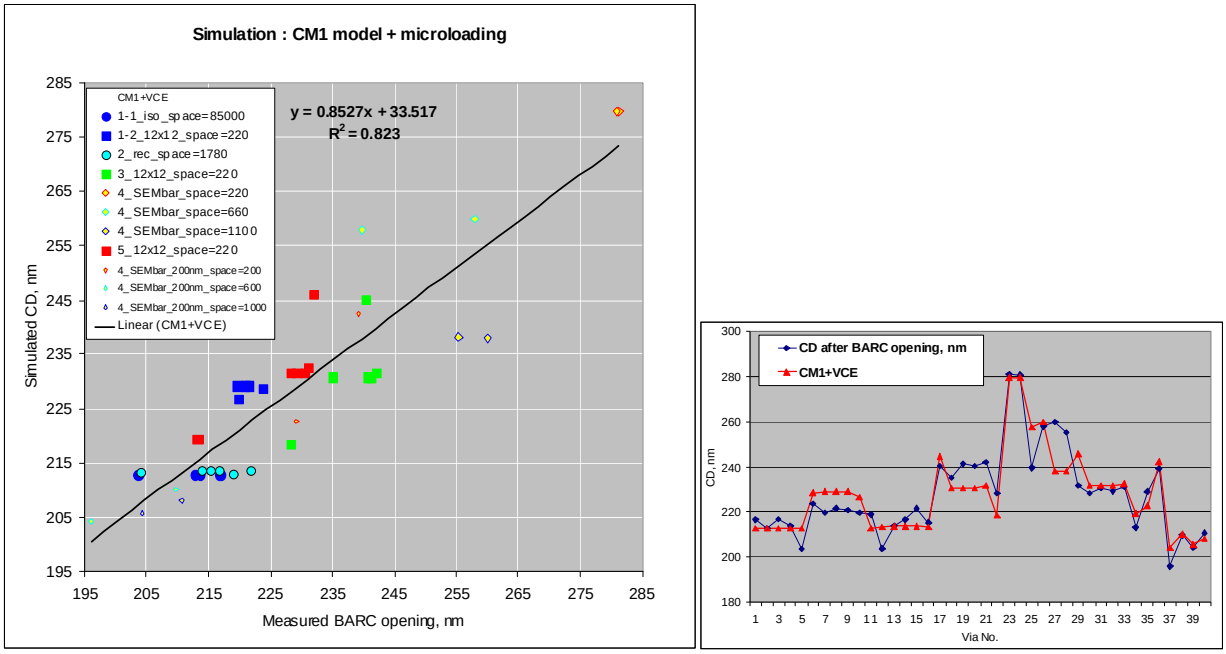

Fig.1. Results of the calibration of BARC etch-step; simulated photo resist openings are used as the top CDs.

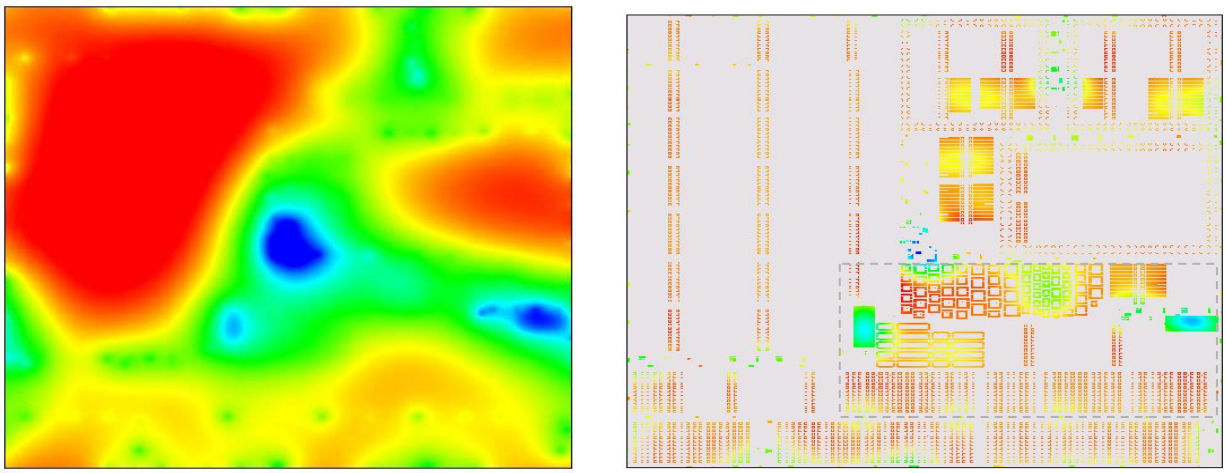

Fig.2. Across-die distribution of the radical flux and the via bottom-CD bias.