E-beam Lithography for Platform of multiple SET architectures

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Within the last decades, transistor dimensions were shrunk to a few nanometres. For those dimensions by modulating the access resistance of the device, it has been demonstrated channel can acts as a silicon quantum dot coupled to the gate and resistive access as a tunnel barrier [1]. Then a standard single gate MOS-FET is a Single Electron Transistor (SET) at low temperature. Coulomb blockade effects have already been studied with silicon architectures, using several gates for modulating tunnel barriers and number of electrons in the dot, as well as for modulating coupling between dots. [2][3]. In the European project AFSID (Atomic Functionalities in Silicon Devices) we propose to build a silicon platform enabling the comparison of single gate MOS-FET as a SET and other architectures (using side gates, constrictions...), and to study coupled SET. For this purpose adapted and performing lithographic processes are required, especially in terms of spacing, then enabling effective gate-to-dot, or dot-to-dot coupling.

We aim to combine single electron transistor, side gated transistor and other alternative architectures on the same wafer. This platform was highly complex to obtain with regard to the device dimensions (Fig. 1) – close to 20nm – and device architectures (Fig. 2). Furthermore, a very accurate alignment control of the different lithography layers was necessary, particularly between the active area and the gate patterning. For this purpose, we used hybrid lithography (e-beam/DUV), via the use of chemically amplified resists (CAR) [4, 5]. The e-beam exposures were carried out on a Gaussian electron beam writer (Leica VB6-UHR from Vistec) operating at 100KeV, allowing to produce a spot size of about 4 nm. In order to reach all the devices on the same wafer we added datatypes and proximity effect corrections were tested.

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- [2] A. Fujiwara et al., Applied Physics Letters 88, 053121 (2006)
- [3] Andrew J. Ferguson et al., Applied Physics Letters, volume 82, Number 25 (2003)
- [4] R.Wacquez, M.Sanquer, M.Vinet, X.Jehl, S.Pauliac-Vaujour, et al., SSDM proc. pp 1082 (2008)
- [5] S. Pauliac, S. Landis, J. Foucher, J. Thiault, Microelectronic Engineering 83 (2006) 1761-1766
- [6] S. Pauliac-Vaujour et al., J. Vac. Sci. Technol. B, Vol. 25, Issue 6, pp. 2030-2033 (2007)



Fig. 1 : Alternative Silicon SET architectures with side gates controlling tunnel barriers or dot potential. Spacing is down to 40nm.



Fig. 2 : Coupled SETs formed by a double constriction and a dot.

^[1] Hofheinz et al APL.89, 143504, (2006).