Resist Residues and Transistor Gate Fabrication

D.S.Macintyre, O.Ignatova, S.Thoms, I.G.Thayne

James Watt Nanofabrication Centre, Department of Electronics and Electrical Engineering, University of Glasgow, Glasgow G12 8LT, Scotland.

In this paper we investigate the formation and removal of resist residues with the main objective to improve the reliability of transistors gate fabrication. Device performance is strongly dependent on the quality of metal contacts and the interface between gate metal and substrates. Reliable transistor fabrication becomes increasingly difficult as transistor dimensions shrink. This is particularly true if wet or dry etching steps are required for gate recessing eg for pHEMTs or the removal of thin oxide layers in III-V MOSFET fabrication and residual resist layers can become significant.

We observe two sorts of residual resist layers in PMMA: exposed and non-exposed. Exposed residual layers have been observed by many groups in electron beam exposed and developed regions of PMMA and in this paper we consider this effect on gate fabrication. We also present evidence of a non-exposed residual layer, observed in regions of unexposed resist which have been subject to a standard solvent based resist strip and cleaning procedure.

Fig 1 shows a 1 kV SEM micrograph of the non-exposed residual layer. A silicon substrate was coated with 100 nm PMMA (MW 80k), patterned by electron beam lithography and developed for 30s in 2.5:1 IPA:MIBK. It was then subjected to an oxygen plasma which removes 10 nm of PMMA, and thus any of the exposed residual layer in the patterned regions. The resist was then stripped in acetone with ultrasonic agitation for 5 minutes followed by a similar treatment in isopropyl alcohol. In the micrograph the light coloured areas are the silicon substrate and the dark areas are non-exposed residual resist left after the resist strip. No roughness is visible within the residual layer. This is confirmed by AFM analysis which reveals that the layer is about 3 nm thick. Clearly, in a multilayer process care needs to be taken to remove this residue.

Maximov et al [1] used XPS to demonstrate that 1 nm of residual resist can remain after electron beam exposure. AFM inspection [2] reveals that this layer can be granular. Here we used AFM to investigate residual resists in gate fabrication. We found that at doses typically used for gate fabrication the exposed residual resist layer is still granular and there is a sub nanometre continuous surface film. This was done by preparing a substrate such that regions of bare silicon were adjacent to regions which were exposed and developed. The results are shown in Fig 2 which also shows fabrication details. The dose used in the exposed region was about 50% above the clearing dose, which is slightly higher than is typically used for gate fabrication. The granularity problem is worse at lower doses and because the residual layer is non uniform it is harder to remove completely, thereby increasing the minimum gate widths which can be achieved.

[1] I.Maximov, A.A.Zakharov, T.Holmqvist, L.Montelius, I.Lindau, J.Vac. Sci. Technol. B 20(3) 2002 pp1139-1142

[2] S.Yasin, M.N.Khalid, D.G.Hasko, Japanese Journal of Applied Physics, 43(10) 2004 pp6984 -6987

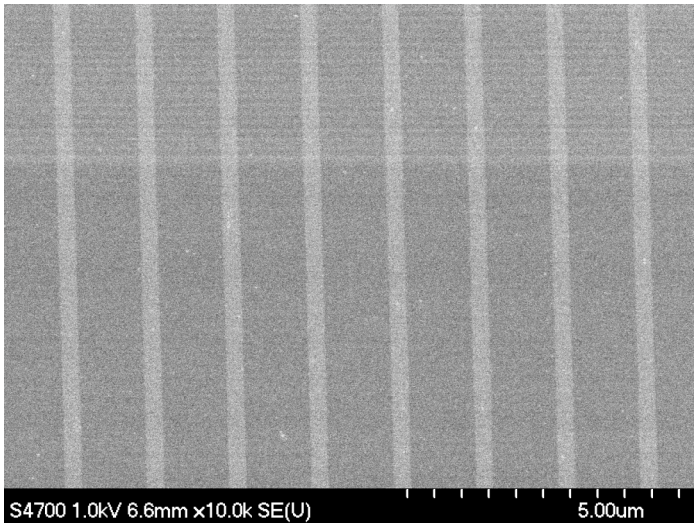

Figure 1. A latent image of PMMA on silicon after patterning a 100 nm thick film, developing in 2.5:1 IPA:MIBK, ashing for 60s at 40W and cleaning off the resist using acetone and isopropyl alcohol with ultrasonic agitation. Dark areas show residual resist in unpatterned areas while light areas are exposed areas after removal of residual resist by ashing.

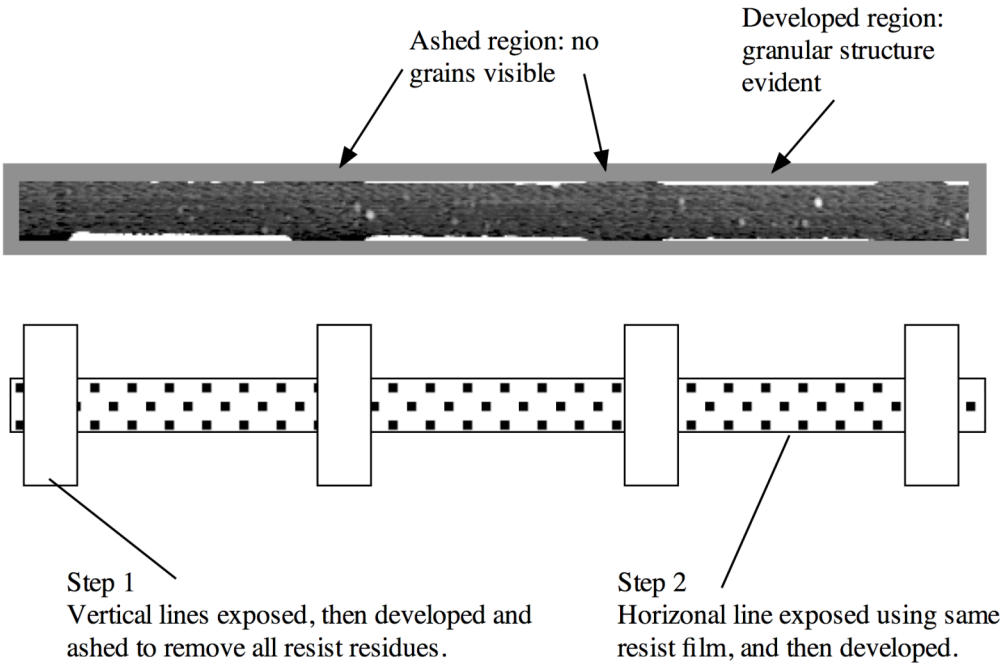

Figure 2. AFM micrograph showing resist residues in exposed and developed regions alongside areas of bare silicon. The granular structures are up to 10 nm thick, and a sub-nm background layer is apparent in the exposed regions.