Design Verification for sub 70 nm DRAM nodes via Metal Fix using E-Beam Direct Write

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ABSTRACT

Because of mask cost reduction, electron beam direct write (EBDW) is implemented for special applications such as rapid prototyping or small volume production in semiconductor industry. One of the most promising applications for EBDW is design verification by means of metal fix. Due to write time constrains, Mix & Match solutions have to be developed at smaller nodes. This study reports on several Mix & Match processes for the integration of E-Beam lithography into the optical litho process flow of Qimonda's 70 nm and 58 nm DRAM nodes. Different metal layers have been patterned in part with DUV litho followed by E-Beam litho using a 50 kV Vistec SB3050 shaped electron beam direct writer. All hardmask patterns were then simultaneously transferred into the DRAM stack. After full chip processing a yield study comprising electrical device characterization and defect investigation was performed. We show detailed results including CD and OVL as well as improvements of the alignment mark recognition. The yield of the E-Beam processed chips was found to be within the range of wafer-to-wafer fluctuation of the POR hardware. We also report on metal fix by electrical cutting of selected diodes in large chip scales which usually cannot be accessed with FIB methods. In summary, we show the capability of EBDW for quick and flexible design verification.

Keywords: EBDW, Mix & Match, E-Beam Lithography, Design Verification, Metal Fix

1. INTRODUCTION

Electron beam direct write (EBDW) is one of the widely accepted technologies for maskless generation of sub 50 nm pattern in semiconductor manufacturing. Even though its low throughput is a major obstacle of productive usage, EBDW is implemented for special applications such as rapid prototyping or small volume production because it can eliminate significant mask costs [1]. Currently, large efforts are spend on acceleration to insert massively parallel Maskless Lithography into IC manufacturing within the European framework of the MAGIC consortia [2].

At the Fraunhofer Center Nanoelectronic Technologies the Center of Competence E-Beam puts these special EBDW applications into practice and provides full customer services starting from the discussion of an integration setup, the process development, execution and optimization, the proximity effect correction and last but not least the optical and SEM inspection. Exposures are performed on the VISTEC Variable-Shaped E-Beam Direct Writer SB3050DW. One of the most promising applications for EBDW is design verification by means of metal fixing. In the past we have successfully demonstrated the integration of EBDW of one entire metal layer as substitution for optical lithography in 220 nm node microcontrollers [3]. This typical example for personalization included customer specific samples, strictly speaking different ROM codes on the same wafer.

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2. MOTIVATION FOR METAL FIX

E-beam lithography offers metal fix options for the Back-End-Of-Line (BEOL) layers on the same wafer, for instance with the preparation of different chip designs, which lead to an appreciable reduction of cycle time and cost together with an increased flexibility [1]. Two problems out of the development area give rise to the application of e-beam metal fix litho:

- Problem 1: A design bug was found in silicon; the redesign requires only the changes of a few layers. This problem is common for radiofrequency chips.
- Problem 2: The timing has to be optimized by means of connectivity variants.

Today the development engineers wait several weeks for a mask redesign and a new tape-out. Therefore, the goal is to write the modified layers with e-beam litho (when the repair option requires only small changes) or to expose only a single or a few layers with e-beam litho and use mix and match. The clear advantage lies in the potential to integrate different redesign versions on one wafer. Beneficial are also the saving of mask costs and the better time to market. For EBDW, the following points are assumed: E-beam litho should align to the optical (standard) litho and should be 100 percent transparent to the designer or customer. Furthermore, it should deliver the same electrical results like the POR.

EBDW needs either the same resist mask for optical and e-beam litho or an equivalent CD after hardmask open (if there are differences in hardmask etching).

3. MIX & MATCH INTEGRATION

Due to write time constrains, full layer printing is not always possible at smaller nodes and Mix & Match solutions for optical litho – e-beam litho have to be developed.

3.1 Integration concepts

An overview of integration concepts is given in Figure 1, left side. The most promising concept besides printing of the entire wafer with e-beam lithography is the printing of full reticle blocks by means of a double patterning approach (Fig. 1, right). The principle here is the sequence litho – etch – litho – etch. The optical exposure is done for all reticle blocks except those to be patterned by e-beam litho (A), followed by the hardmask open process (B). The remaining reticle blocks are now exposed with e-beam (C), followed by the second hardmask open step (D). The joint hardmask patterns are then simultaneously transferred into the underlying DRAM stack by the main etch (E).

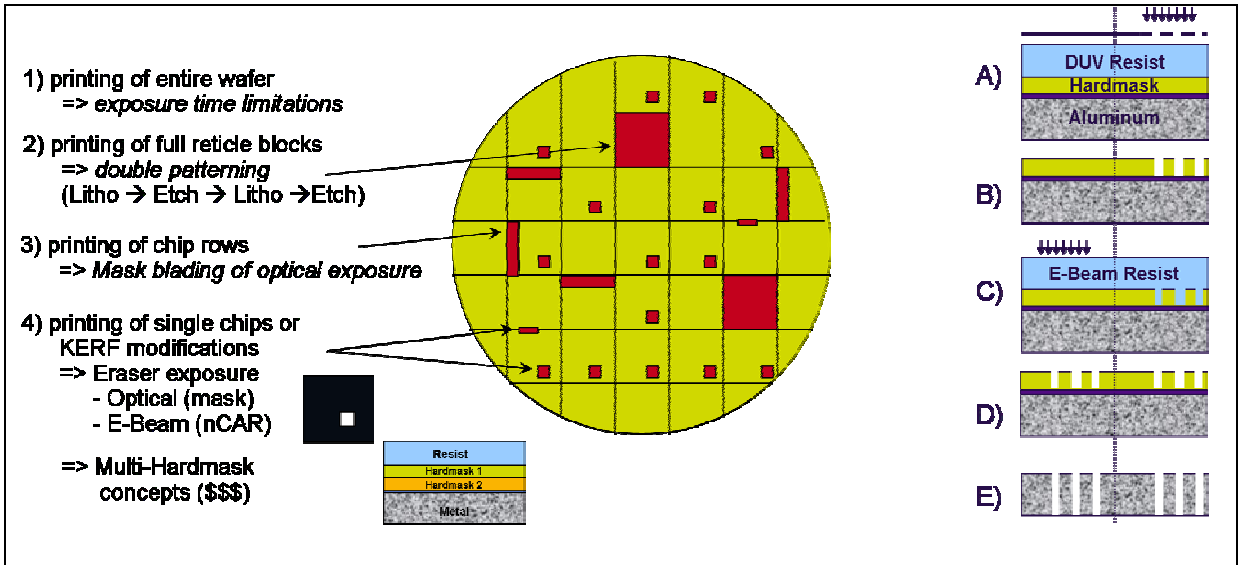

Fig. 1: Different integration concepts for mix and match of optical litho – e-beam litho (left); Double patterning (right)

The third integration concept consists of the printing of chip rows, which can be achieved by mask blading of the optical exposure. The last concept is used for the printing of single chips or KERF (dicing frame) modifications. This scenario works with an expensive multi-hardmask approach, but still has to be established for the usage of an optical mask to "erase" the area to be printed with a negative e-beam resist.

3.2 E-beam alignment setup

For every integration concept a specific alignment has to be set up in which e-beam lithography has to align to the optical litho and/or the underlayer. Typically, a global alignment is followed by a precise local (chip) alignment. Both should preferably not damage the ambient chips in the consecutive process steps; the exposed and thereby corrupted resist area is to be kept as small as possible to still ensure sufficient alignment accuracy.

In Fig. 2, during global mark exposure the optimization of the alignment mark scanning prevents any chip damage. In Fig. 3, the optimization of the mark scan reduces the corrupted mark area during local mark exposure.

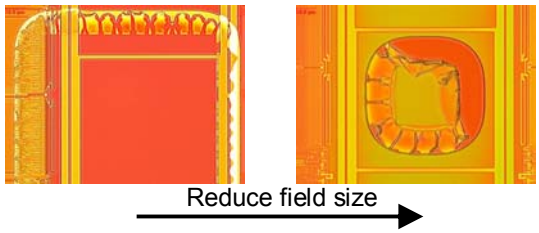

Fig. 2: Optimized global mark exposure

Fig. 3: Optimized local mark exposure

3.3 Comparison of e-beam and optical litho

After exposure and metal etch, the structures generated by e-beam and optical litho were compared by means of optical inspection as well as SEM and AFM measurements. No significant differences were observable between e-beam and optical exposed reticle blocks. The heights of selected structures were comparable; also the CDs of isolated and nested features did not differ between the exposure technologies.

To avoid any blocking points regarding contamination, a detailed defect investigation was performed. The defect density of the entire area of each wafer was determined post main etch. Surprisingly, the e-beam reticle blocks showed a similar or even lower defect level then the reticle blocks exposed by optical litho. Only some bridging between the lines occurred, which was related to optical litho and hardmask etch.

4. METAL FIX APPLICATIONS

With the developed Mix & Match integration schemes, several metal fix projects where realized together with Qimonda Dresden. Different metal layers have been patterned in part with e-beam / optical double patterning lithography, depending on the desired change of the layout. Some selected examples are introduced in the following.

4.1 Yield demo for 70nm DRAM

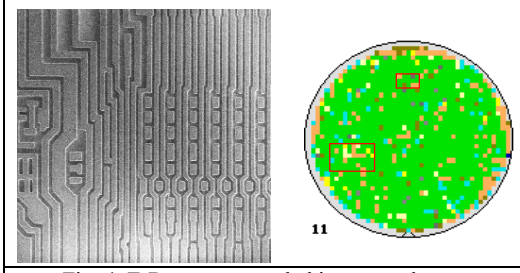

Fig. 4: E-Beam patterned chip area and full wafer yield map.

The wafers received the optical litho process of the first metal layer except for five reticle blocks. After the hardmask open, these five blocks were patterned with e-beam and then the joint hardmask patterns where simultaneously transferred into the underlying DRAM stack. After full chip processing, the electrical device characterization showed the functionality of the e-beam chips; more than 100 operational components have been generated with e-beam litho. Their electrical yield was found to be within the range of wafer-to-wafer yield fluctuation of the POR hardware (Fig. 4).

4.2 E-fuse patch for 70nm DRAM

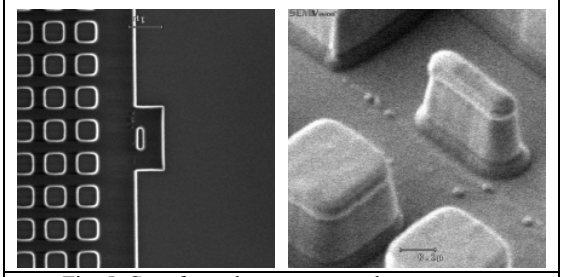

Fig. 5: Cut of metal area to cover the contact.

This metal fix consisted of the generation of "breaks" for electrical fusing. A cut of the metal area was exposed in such a manner that "islands" were left to cover the underlying contacts. With this repair option, two entire lots where exposed, each with 384 chips per wafer. The electrical tests showed significant yield improvements (Fig. 5).

4.3 Redesign for 70nm DRAM

The third application is an example for design verification. Against the background of a slew rate test before mask tape-out, two different design options were integrated into the wafer process flow. E-beam lithography acted here as a substitute for focused ion beam (FIB), but with improved statistical yield. In optical lithography, two designs of one wafer are only possible with a more complex shared reticle approach.

4.4 Diode cut-off for 58nm DRAM

As a countermeasure for an input leakage issue, a secondary electro-static discharge diode cut off was provided by e-beam lithography. The generated components were needed for a customer validation.

17 times 852 chips were modified, which means a total number of 80088 metals cuts per wafer. Through this fast and flexible e-beam approach, only ten days were needed from the customer request until the delivery of the wafers. Using a conventional method would have been factors more expensive.

5. SUMMARY

In summary, the capability of EBDW as a viable and flexible method for quick design verification was demonstrated. Several metal fixes have been implemented with e-beam lithography into the optical litho process flow of Qimonda's 70 and 58 nm DRAM nodes within the last two years. The electrical comparison between chips exposed by either optical or e-beam litho showed no performance differences. The e-beam metal fixes hold its major improvements in cost and speed compared to conventional methods. It is even possible to run a metal fix by means of electrical cutting of selected circuits or diodes in large chip scales which usually cannot be accessed with commonly used FIB methods.

The design rule learning is a subject of further studying.

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