Parallel Proximal Probe Arrays with Vertical Interconnections

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Massively parallel operation of large arrays of Scanning Probe Sensors makes possible a higher imaging throughput. Real parallelisation can be achieved properly with an individually actuated and sensed Scanning Probe Sensors. The project described here builds on prior works done in the frame of the European project “Pronano” and presented at this conference (EIPBN 2008), where aluminium planar interconnections were employed [1].

In this work we are presenting a low-resistance polysilicon electrical through-wafer interconnects (ETWI), which, have been integrated with the piezoresistive deflection sensor and bimetal (bimorph) actuator to enable backside contacts to the drive ASIC circuitry. The interconnects were fabricated in a fully complentary metal–oxide–semiconductor (CMOS) compatible process using a gas chopping based deep reactive ion etch (GChDRIE) [2], producing a 30μm diameter, high aspect ratio through-wafer vias on a SOI wafer (Fig. 1) and then refilled with highly doped polysilicon (Fig. 2). The formation of the cantilevers incorporates the formation of silicon membranes which are etched using the same (GChDRIE) plasma based etching technique (Fig. 3). The influence of the electrical interconnection in terms of the overall performance of the cantilever array have been shown and investigated, which makes ETWI recommended [3]. We present a new fabrication sequence for integrated-silicon microstructures designed and manufactured in a conventional CMOS process. We will demonstrate the ability to fabricate small through-wafer electrical interconnections having broad application fields for integrated circuits and micromachined devices.

For the realisation of one dimensional (linear) cantilever arrays, the cantilevers approach the sample at an angle so that the cantilevers can be flat. In case of 2D cantilever arrays, the cantilevers have to be pre-bent and the AFM-tips are placed 15 to 30 microns above the chip level (Fig. 4) [4].

Here we will present the performance characteristics of such two-dimensional micromachined silicon cantilever arrays with integrated through-wafer poly-silicon electrical interconnect. An AFM imaging employing hybrid electronic circuitry is used for the cantilever characterisation with respect to prepare optimal ASIC chips design.

Fig. 1 Cross-section of through-wafer etched via. The etching is stopped on the SIO2 layer.

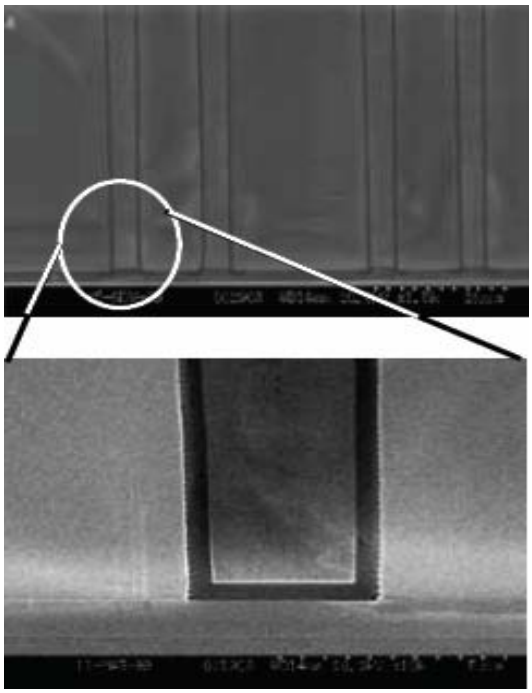

Fig. 2. Cross-section of fabricated SOI-wafer with vertical interconnections. Picture represents the interface of the poly-silicon column and Silicon top layer of the SOI-wafer.

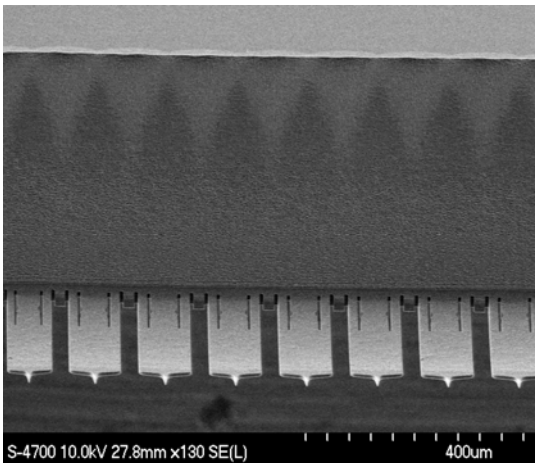

Fig. 3 Detail of cantilever array formed by dry etched SOI-wafer (back side view).

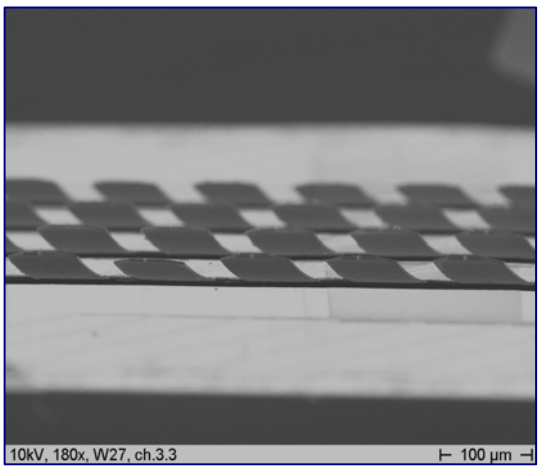

Fig. 4 Array of pre-bended Cantilever

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[2] I.W. Rangelow, J. Vac. Sci. Technol. A 21.4., p. 1550, 2003
[3] A. Frank *at all*., Proceedings Eurosensors XXII, Dresden, Germany, 7-10. Sept., 2008
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