High performance lithographically defined back-gated Si-nanowire MOSFETs with sub-5 nm channel width

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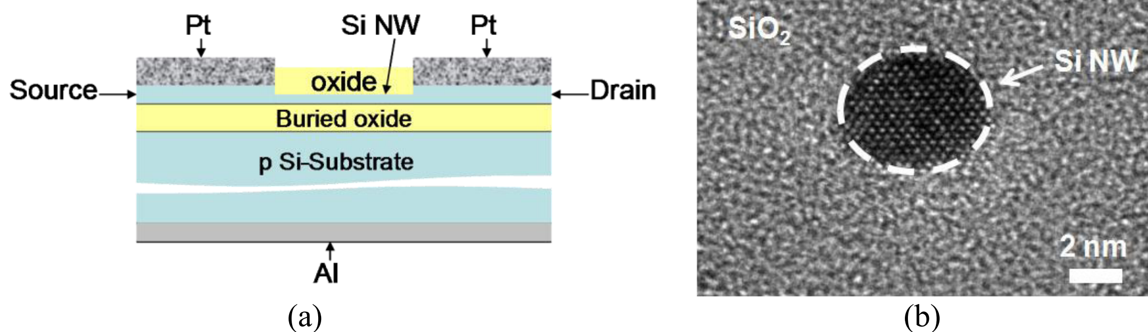
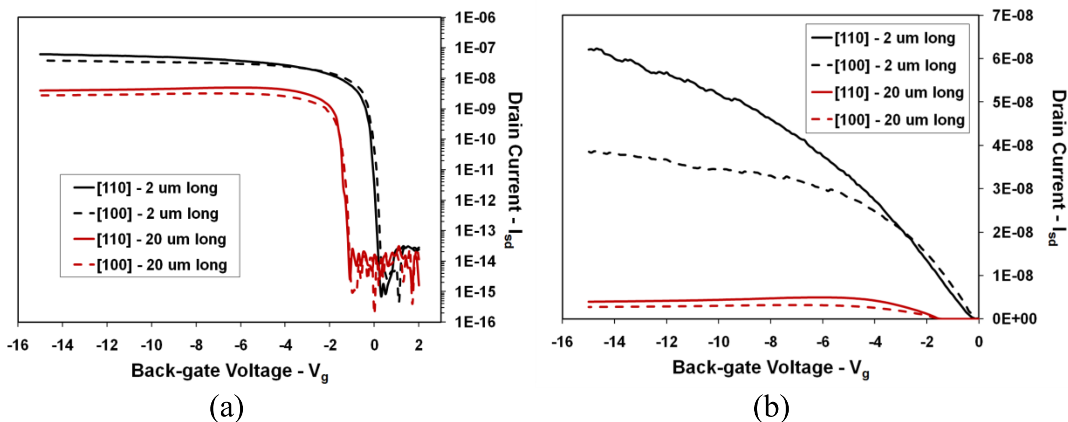
Nanowire field effect transistors (NWFETs) are emerging as important devices, poised to play a significant role in both extending performance of scaled silicon CMOS as well as application in biochemical sensing. Concepts such as FINFETs already demonstrate the feasibility of lithographically defined sub-20 nm nanowire short channel devices in CMOS configurations. For biochemical sensing, long channel NWFETs with back-gate configuration are typically employed. Smaller nanowires are desired for better device performance and higher sensitivity in biochemical sensing. It is believed that NWFETs with sufficiently small nanowires (sub-5 nm) may exhibit quantum confinement, resulting in effects like increased carrier mobility and undesirable mobility oscillation or degradation of performance due to increased surface scattering. Understanding of such effects is critical for the design of nanowire devices for advanced performance, e.g. ultra-sensitivity in biochemical sensors. Bottom-up techniques such as chemical vapor deposition (CVD) have been the mainstream method to grow small nanowires with better resolution than lithography. However, the lack of control over size, doping, contamination, along with device fabrication/integration issues inherent to bottom-up techniques have resulted in poor device reliability and reproducibility.

In this study, we present reliable fabrication of back-gated NWFETs with lithographically defined sub-5 nm nanowires that are comparable in size to CVD nanowires. We investigate transfer characteristics and mobility behavior of sub-5 nm channel width P-MOSFETs as a function of channel length and crystal direction. As shown in figure 1a, the devices are fabricated atop an ultrathin p-type (10^{15} cm^{-3}) silicon-on-insulator wafer with 10 nm top Si (Siltron, Korea). The nanowires are first defined by e-beam lithography in HSQ resist and plasma etching, followed by thermal oxidation to precisely reduce nanowire dimension (fig 1b). Devices with nanowires of lengths between 2 and 20 µm and cross section as small as 3 - 4 nm are made in both [100] and [110] directions. The NWFETs are completed with deposition of aluminum on the backside silicon for back-gate and platinum on un-doped source/drain pads, forming schottky contacts, thereby greatly simplifying the overall fabrication process. Figure 2 shows transfer characteristics (I_{sd}-V_g) and Figure 3 shows calculated field effect hole mobility of sample nanowire P-MOSFETs. These tiny devices have shown excellent performance (On/Off ratio>10^6, sub-threshold slope ~70mV/decade, gate leakage current <10^{-11}A) with considerably high mobility (~100 cm^2/Vs). Threshold voltage of 20 µm length channel devices is lower than 2 µm length devices. Drain current saturation is observed for 20 µm at a lower back-gate voltage. Quantum confinement induced mobility oscillations are observed at room temperature only at higher back-gate fields. The mobility increases with increasing channel length, suggesting transconductance of these NWFETs does not scale with length. This approach enables reliable fabrication of back-gated sub-5 nm channel width NWFETs with applicable electrical performance, at low gate fields.



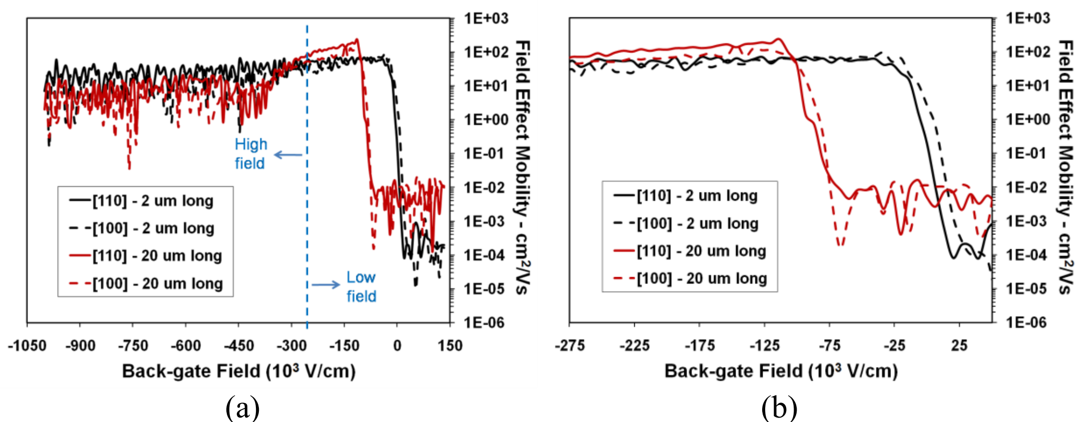
(a) (b)

Fig 1: (a) Schematic of a Si-nanowire P-MOSFET device and (b) a TEM image of the cross section of a lithographically defined Si nanowire after oxidation.



(a) (b)

Fig 2: Transfer characteristics (I_d-V_g) of back gated Si nanowire P-MOSFET devices in (a) log and (b) linear scales. All devices have nanowires with cross section of less than 5 nm.



(a) (b)

Fig 3: (a) Calculated field effect mobility of Si nanowire P-MOSFET devices and (b) a zoomed-in view of the same field effect mobility for low gate fields.