Very high aspect ratio fabrication process for stacked nanowire transistors with gate-all-around (GAA) or double-gate (ΦFET)

S. Pauliac-Vaujour, P. Brianceau, C. Comboroure, N. Lamard, C. Vizioz, S. Barnola, V. Maffini Alvaro, A. Hubert, C. Dupre, T. Ernst, P. Sixt
CEA/LETI - Minatec, 17 Rue des Martyrs, F-38054 GRENOBLE Cedex 9, France, e-mail : sebastien.pauliac@cea.fr, pierre.brianceau@cea.fr

Stacked nanowire metal oxide semiconductor field effect transistors (MOSFETs) with gate-all-around (GAA) or double-gate (ΦFET, patent EN 07 57 690) are well known for being potential candidates for sub-32nm nodes [2], thanks to their excellent electrostatic control combined with a high on-current (I_{ON}) [1-3]. Furthermore, we have already demonstrated that their power consumption could be reduced by using independent gate architectures (ΦFET) [4] (Fig.1).

The stacked nanowire transistor fabrication is highly complex with regards to lithography and etching, especially during active area definition. During our first experiments, we yielded 18nm stacked nanowire MOSFETs with gate-all-around and for the first time [5-7], we succeeded in achieving sub-20nm ΦFET devices (Fig.1) via the use of an hybrid lithography (e-beam/DUV) and resist trimming process [6, 7]. Moreover, the ΦFET electrical results are excellent: for *n*MOS transistors, I_{ON}=6.5mA/µm and I_{OFF}=27nA/µm at an input tension V_{DD}=1.2 V; and for *p*MOS, these values are I_{ON}=3.3mA/µm and I_{OFF}=0.5nA/µm (V_{DD}=1.2 V). These results have been achieved with a Si/SiGe multilayer stack of thickness 200nm which corresponds to 4 stacked nanowires. However, for improving their current density per layout surface we must increase the number of stacked nanowires. Hence the need to develop a 1µm Si/SiGe process in order to multiply by 5 the number of nanowires.

For succeeding to etch a 1µm Si/SiGe multilayer stack, a high aspect ratio hybrid resist process was performed (Fig. 2), using a chemically amplified resist (NEB22), an ASML stepper (wavelength: 248nm) and a Vistec100KeV Vector beam (Fig. 2) [5-6]. Thanks to this thick resist, we are able to open a 300nm thick oxide hard mask (Fig. 3(A)) keeping the CD bottom of the oxide lines the same as the original lithography CD. Then, the oxide hard mask gives us the opportunity to reach more than 1µm Si/SiGe multilayer stack (Fig. 3(B)) due to an excellent Si/SiGe selectivity to oxide. In this example, we succeeded to etch a stack composed of 13 layers of SiGe (25nm) and 12 layers of Si (30nm) which gives a stack of 1015nm.

[1] T. Ernst et al., IEDM Techn. Digest 2006, p.997
[2] A. Hubert, C. Dupré, T. Ernst, S. Pauliac et al., ECS Trans. 13, (1) 195 (2008)
[3] Y. X. Liu et al., IEEE Int. SOI Conf. 2005, p. 219
[4] C. Dupré et al., IEEE International Electron Devices Meeting IEDM 2008
[5] S. Pauliac-Vaujour et al., J. Vac. Sci. Technol. B26(6), p2583 Nov/Dec 2008
[6] S. Pauliac-Vaujour et al., J. Vac. Sci. Technol. B, EIPBN09 (in press 2010)
[7] S. Barnola et al, ECS Transactions, 16 (10) 923-934

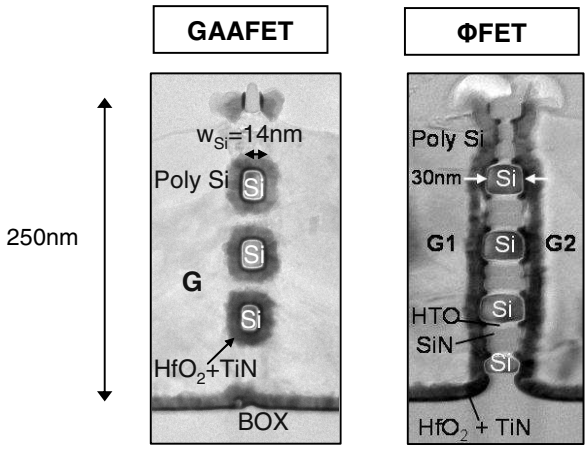

Fig 1. Cross sectional TEM images of stacked nanowire MOSFET gate-all-around (GAAFET) and double-gate (ΦFET)

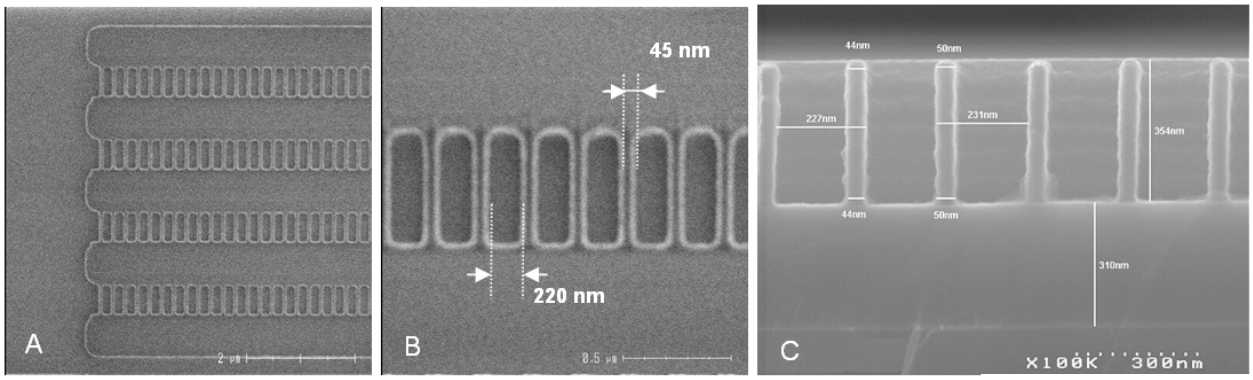

Fig. 2: Top SEM view of the active area hybrid lithography (A, B), Cross sectional SEM view of resist patterns (thickness: 400nm) (C)

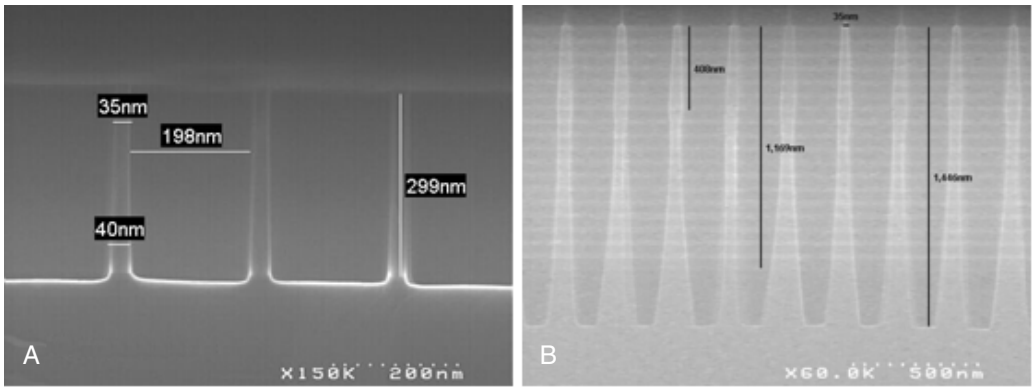

Fig. 3: Cross sectional SEM views of the oxide hard mask (A), and of the 1015nm Si/SiGe stacked nanowires etched up to 1.6µm (no oxide stopping layer) (B)