SINGLE-STEP, WAFER-SCALE, HERMETIC SEALING USING SILICON MIGRATION

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We have demonstrated a new single-step, wafer-scale process for sealing release holes in micro- and nano-structures based on silicon migration. Our technique will enable the fabrication of a variety of micro- and nano-devices where it is desirable to use release holes to free structural parts during the fabrication process even though the final structures must have only large, flat, continuous surfaces without holes in order to function properly - for example, absolute pressure sensors and micro-mirrors. Additionally, hermetic packaging of micro- and nano-devices can be another promising application for our use of silicon migration (Figure 1).

Silicon migration is a surface phenomenon that occurs on crystalline silicon at 900-1100°C in wide range of ambient environments [1,2]. This phenomenon arises from the tendency for silicon to minimize surface energy through physical migration of surface atoms, which leads to significant shape transformations such as planarization of surfaces, rounding of edges and the splitting or joining of interfaces [1,3].

We leverage this shape transformation to create robust and continuous membranes that maintain hermetically sealed environments. We chose two release hole designs for our study: 0.62um diameter circular holes with a 1um pitch, and 0.99um long square holes with 1.5um pitch. One 100x100um area and four 200x200um area arrays of each release hole design (10 devices total) were patterned and etched through the 2.96μm device layer of an SOI using RIE. Buffered HF was used to etch the buried oxide. Finally, silicon migration was induced at 1100°C for 40minutes in 10Torr H_2. Before and after SEMs (Figure 2a,b) confirmed the formation of continuous sealed membranes from the perforated structure. 30kV SEM showed the presence of the trapped voids under the surface (Figure 2c). An 80-degree tilt view showed a thickness difference between the initial device layer and the final membrane (Figure 2d).

We developed a custom 3-D simulator to model the effect of silicon migration for our experimental structures [3]. The arrays were modeled as a single hole with periodic boundary conditions. The simulation predicted that the openings would close on both sides leaving a trapped void within the silicon membrane (Figure 3). The predicted thicknesses of the final membranes were 2.5um and 1.7um for the circular and square hole designs respectively. Additionally, the simulator predicted that a step height would form at the membrane edge - 0.23±0.02um for circular holes design and 0.63±0.05um for square holes design, which were within 10% of the values measured by AFM.

Because the vents were sealed in 10±2Torr H_2, there exists a 750±2Torr pressure difference across the membranes between ambient air and the trapped H_2 ambient that causes membrane deflection. The membrane deflection was measured using white light interferometry (Figure 4). The membrane thickness values were derived from the deflection for both designs and compared to simulation results in Table 1. Both step height and membrane thickness values were within 10% of projected values.

The membrane deflections were re-measured after 60 days and 210 days. After 60 days, the deflection did not vary outside of the measurement error for all 10 devices. After 210 days, 9 of the 10 devices still maintained the initial vacuum indicating that their pressure leakage was below the measurement threshold of 0.18Torr/day (threshold calculated as pressure difference corresponding to 3σ deflection change / 210 days). Our data demonstrates that the sealed membranes are robust and can be used for hermetically packaging micro-structures.

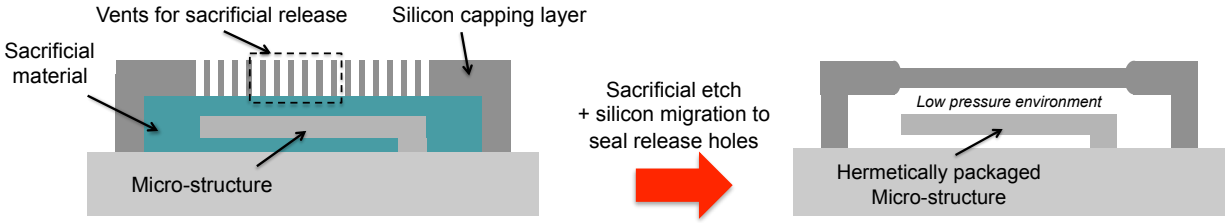

Figure 1: Sketch of potential hermetic packaging application using silicon migration based sealing.

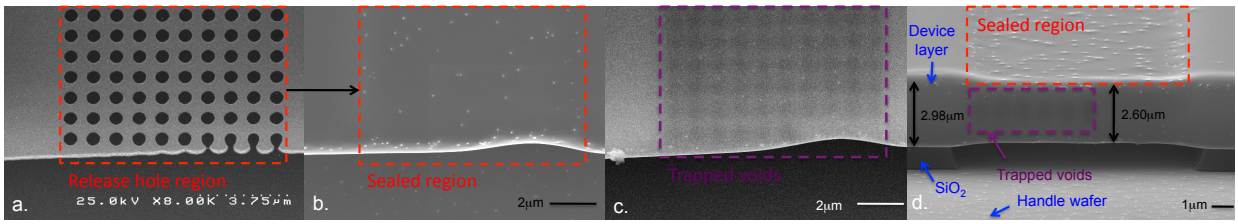

Figure 2: SEM images: (a) Top-view of circular release holes before silicon migration. (b) Top-view of same region at 5kV after migration confirms continuous surface. (c) Top-view of same region at 30kV shows faint outline of trapped voids under the surface. (d) 80-degree tile view of same region shows thickness difference between initial device layer and area where release holes were present, and also shows faint outline of voids.

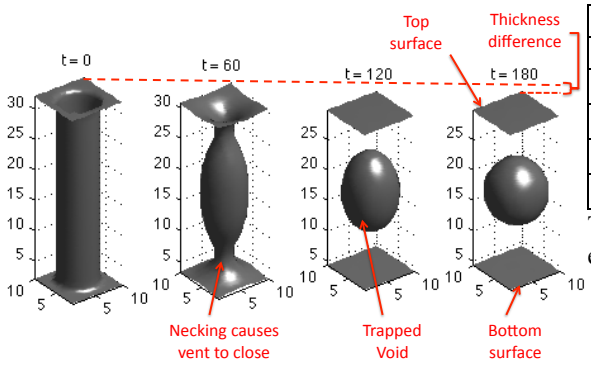

Figure 3: 3D Simulation of circular release holes undergoing silicon migration to form a continuous membrane with a trapped void in between.

	Circular	Square
# devices (Yield %)	5 (100%)	5 (100%)
Step height (sim)	0.23±0.02µm	0.63±0.05µm
Step height (exp)	0.26±0.02µm	0.65±0.06µm
Thickness (sim)	2.5±0.10µm	1.70±0.16µm
Thickness (exp)	2.6µm	1.85µm

Table 1: Comparison of simulation results (sim) to experimentally derived values (exp).

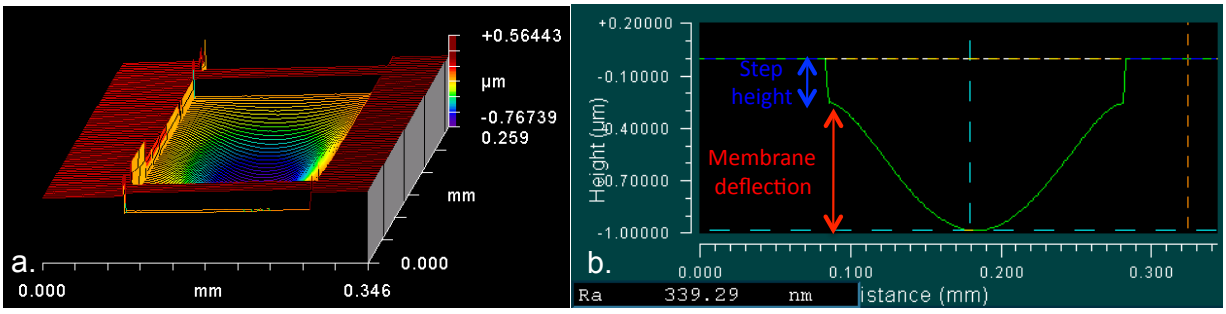

Figure 4: White light interferometer measurement of deflection on a 200x200um area sealed membrane for the circular release hole design. (a) Oblique view of deflection. (b) Deflection measurement through device center.

References:

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