Self-aligned Epitaxial Graphene MOSFETs with a record field-effect mobility of 6000 cm^2/Vs on 50 mm wafers

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Graphene has attracted a lot of attention in the research community as a potential candidate for high performance RF electronics materials. [1] While it has the highest carrier Hall mobility of >100,000 cm^2/Vs at room temperature [2], the saturation velocity (Vsat) of graphene is expected to be two to four times faster [3] than that of lattice-matched InP HEMTs, the current material of choice for high-speed RF applications. A potential combination of high current-carrying density, transconductance and low access resistance could make graphene an attractive candidate for high-performance RF applications. So far, the epitaxial graphene MOSFETs [4-5] are in early stage of development and has shown technical challenges; the current-voltage characteristics are quasi-linear with weak saturation behaviors and low transconductance per capacitance (less than 100 mS/mm at 3.4 fF/μm^2). Also the I_{on}/I_{off} ratio has been <10. While epitaxial graphene RF FETs with fmax of 14 GHz per 2 μm gatelength were demonstrated in a self-aligned top-gated layout with the highest-ever on-state current density of 3 A/mm at Vds = 5 V [5], the field-effect mobility was limited below 200 cm^2/Vs. Most importantly, wafer-scale graphene FETs have yet to be reported.

In this talk, we present a recent breakthrough in epitaxial graphene n-MOSFETs and p-MOSFETs. The epitaxial graphene MOSFETs are fabricated on 50 mm wafers with simultaneous world' record performance in key device parameters for the first time: excellent I-V saturation behaviors, field-effect mobility of 6000 cm^2/Vs for electron with I_{on}/I_{off} ratio of 19, and the peak transconductance of 600 mS/mm. The graphene MOSFETs have been fabricated using standard lithography techniques on epitaxially-grown graphene on 50 mm 6H-SiC semi-insulating substrates. The epitaxial graphene is grown by Si-sublimation of Si-face 6H-SiC substrates in a commercial Aixtron VP508 epitaxial reactor. The number of graphene layers is confirmed by Raman and TEM (Transmission Electron Microscopy). The quality of graphene is characterized by Hall effect characterization prior to the processing.

The graphene RF MOSFETs are fabricated with a gate oxide layer and metal gate stack. Ambipolar behaviors are observed with n-type MOSFET at Vgs = 0 V, while p-type behaviors are observed at Vgs < -1.5 V. The extrinsic field-effect mobility of 6000 cm^2/Vs for electron is obtained at effective electric field of 0.5 MV/cm with I_{on}/I_{off} ratio of 19 at Vds = 50 mV. The measured graphene field-effect mobility is 8-10 times higher than that of ITRS Si n-MOSFETs and ~80 times higher than that of ultra-thin body SOI n-MOSFETs. While the understanding of detailed scattering mechanisms is in progress, we will discuss the graphene field-effect mobility versus the electric field, and compare the trend with universal mobility curves of Si MOSFETs. The epitaxial graphene MOSFETs exhibits I-V curves with excellent current-saturation behaviors for both n-channel and p-channel operations. Based on gm/Cg, the saturation velocity is expected to be several times than that of Si n-MOSFETs. Graphene FETs with a shorter gate length will be discussed. This work was supported by DARPA's CERA Program, monitored by Dr. Michael Fritze under SPAWAR contract number N66001-08-C-2048.

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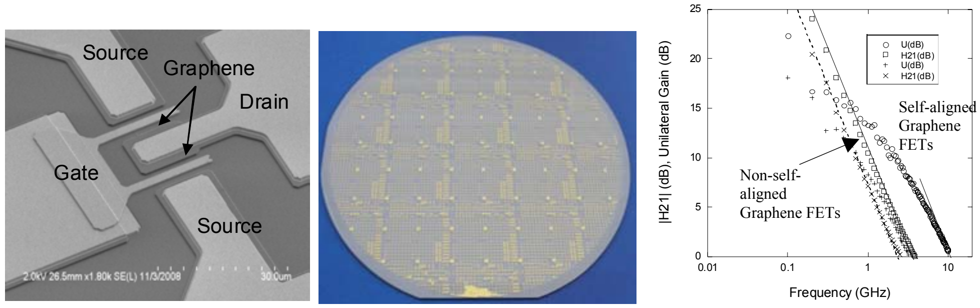

Figure 1. (a) A SEM photograph of the 2 x 12 μm graphene FETs is shown. The gate length is 2 μm. (b) An optical photograph of 50mm graphene wafer processed in standard lithography techniques. (c) Measured magnitude of extrinsic H_{21} ($|H_{21}|$) and unilateral gain (U) are shown as a function of frequencies in self-aligned 2 x 12 μm graphene FETs with Vds = 6 V and Vgs = -2.5 V.

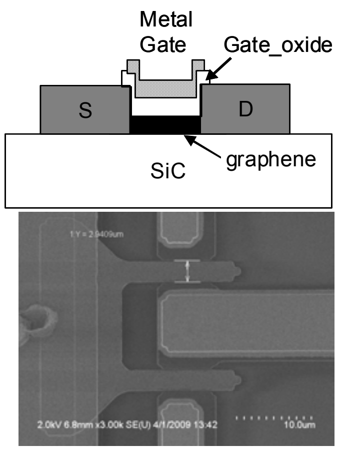

Figure 2. (a) A schematic of the top-gated graphene MOSFET is shown. (b) A SEM photograph of self-aligned 2 x 6 μm graphene FETs is shown. The gate length is 3 μm.

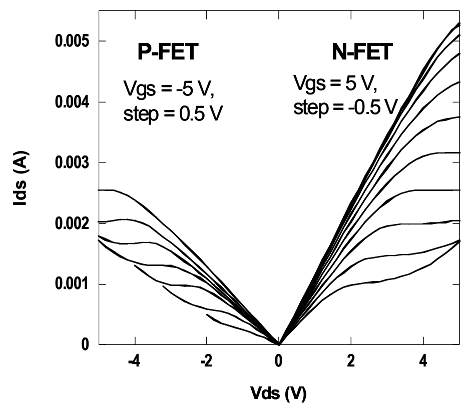

Figure 3. Measured I-V curves of epitaxial graphene MOSFETs are shown with operations for both n-FETs and p-FETs with W = 4um and L = 3um, showing excellent I-V saturation behaviors.

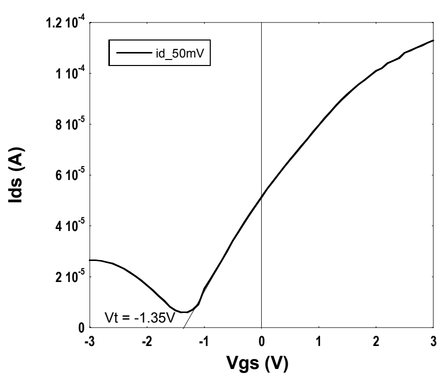

Figure 4. (a) Measured transfer curve of epitaxial graphene MOSFETs at Vds = 50 mV is shown with an ambipolar behavior. The threshold voltage for n-channel FETs is -1.35 V. The Ion/Ioff ratio is 19.

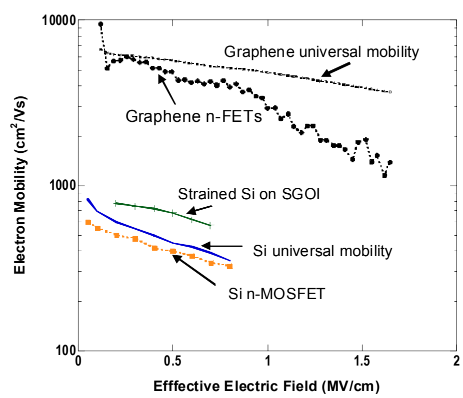

Figure 5. Measured effective mobility and field-effect mobility of graphene n-MOSFETs are shown in comparison with those of Si n-MOSFETs and strained Si on SGOI. The graphene n-MOSFETs have 8-10 times higher mobility than that of Si n-MOSFETs.