Rapid laser crystallization of semiconductors for three-dimensional integration

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Three-dimensional (3D) integration of semiconductor devices can yield advantages in circuit density, power consumption, and speed over conventional integrated circuit (IC) technology in which all transistors are fabricated in one plane. 3D integration allows circuit functions to be split across multiple layers, which – for certain kinds of circuits – allows significant reductions in average wire length. Since wires are the dominant factor in determining logic delay, this can result in faster systems. Vertical interconnect densities of more than a million per square millimeter are critical to achieving this advantage [1], and to do this, a monolithic approach is required where circuit layers are fabricated sequentially on a single wafer.

The principal challenge is obtaining single-crystal, device-quality semiconductor material on upper circuit layers. We show that, beginning from an amorphous silicon film deposited at low temperature on an amorphous silicon dioxide substrate, a rapid laser crystallization process using a 532nm Nd:YAG laser [2] can form preferentially oriented crystals with a <001> out-of-plane orientation. Strong orientation was achieved with pulse lengths 2ms and greater and with 200nm thick silicon films. By patterning the amorphous silicon film into neck structures prior to laser crystallization, a single <001> crystallite can be selected to seed a finger region 10μm in length and several microns wide. Electron backscatter diffraction (EBSD) imaging was used to measure out-of-plane crystal orientation, and shows the seeding effect in detail (Fig. 1(a)). In order to measure carrier mobility, Hall effect devices were fabricated from individual silicon fingers (Fig. 1(b)). Hall mobility was above 900 cm^2/Vs for electrons and 250 cm^2/Vs for holes, and was comparable to SOI reference material (Fig. 2). A forming gas anneal (FGA) was found to markedly improve carrier density in both *n*- and *p*-type devices, and mobility in *p*-type devices. *n*-type devices with mobilities above 600 cm^2/Vs were found to be generally single-crystalline, while lower mobility devices contained multiple grain boundaries.

These crystallized silicon fingers could be used for fabrication of devices, or as seed material for further crystallization. A technique such as rapid melt growth (RMG) of silicon or germanium could be used to crystallize device material and propagate the seed orientation over an entire die. Simulation shows that this could be done without damaging circuit layers underneath, by maintaining their temperature below 400°C. A reflective shield layer and a thermal isolation layer such as silicon dioxide several microns thick are required. The combination of preferentially oriented seed crystallization with an RMG approach would allow the fabrication of multiple circuit layers on a single wafer in a sequential, monolithic fashion.

[1] M. Lin et al, "Performance benefits of monolithically stacked 3-D FPGA", IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems 26 (2007) p. 216.

[2] D. J. Witte et al, "Preferential orientation effects in partial melt laser crystallization of silicon", J. Vac. Sci. Technol. B 26 (2008) p. 2455.

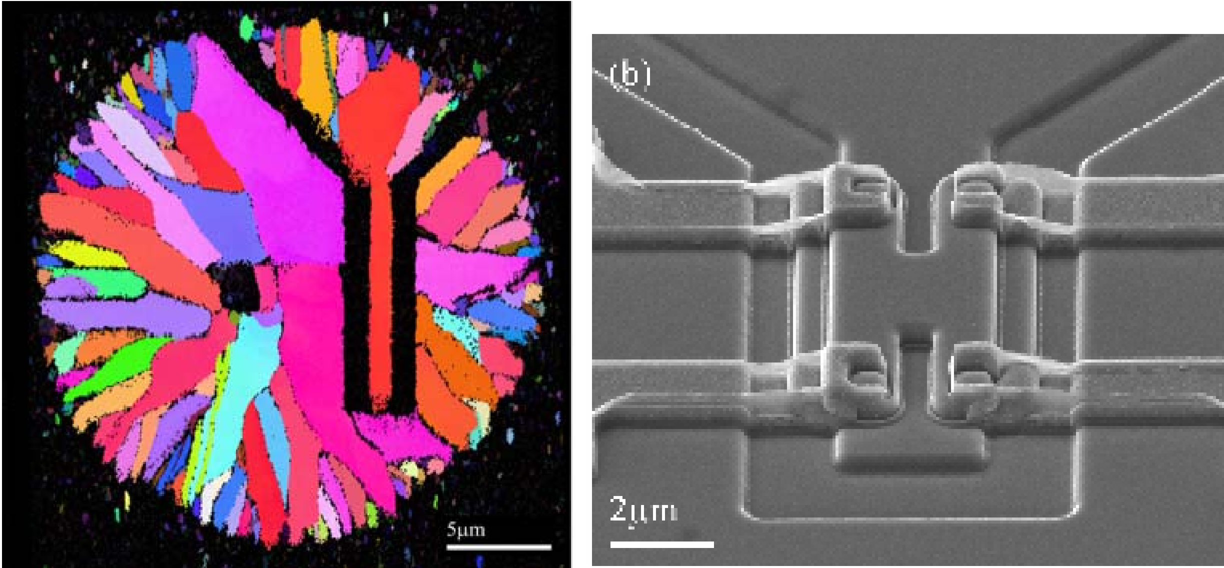

Fig 1: (a) Electron backscatter diffraction image of a 1×10μm finger after laser exposure, showing crystal orientation. Finger region is <001> out of plane. (b) SEM image of a completed Hall device, taken at 52° tilt. Silicon finger is 3μm wide.

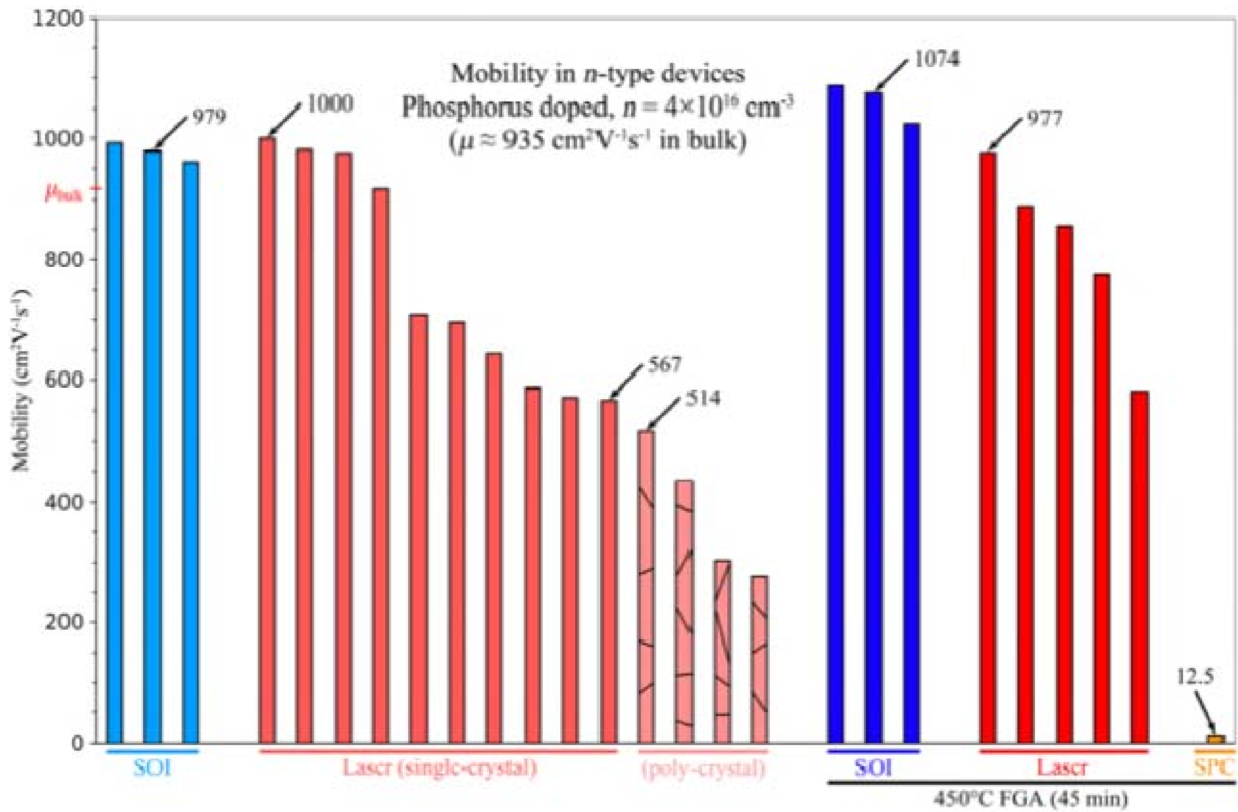

Fig 2: Hall mobility for n-type devices with $8{\times}10^{11}$ cm^{-2} phosphorus dose, showing SOI reference devices and laser-crystallized devices both before and after FGA.