Optical beam steering systems started by mechanical beam directing and stabilization mechanisms, which is subject to limitations such as slow scanning speed (~KHz). Fast Optical Phased Array (OPA)-based optical beam steering systems were first implemented using nematic crystal (LC) cells pioneered by Paul McManamon [1]. The limitations of these devices, such as limited steering angles (<5°) were discussed in details in [2]. We have proposed Silicon-on-Insulator (SOI)-based large steering angle and agile beam steering OPA devices as shown in Fig. 1 [2].

Fabricating the basic waveguides is within the state of the art of current technology. That is, we need to pattern 350nm thick silicon single crystal with lines that are 500nm wide. For our application the required tolerance on the waveguide width variation is not yet completely understood but usually a waveguide width tolerance of wavelength (in the Si)/50 should be adequate. This comes to about 10nm so is just within the capabilities of nano-imprint fabrication techniques and present day optical lithography, respectively, and well within the capabilities of electron beam (Fig. 2). The spacing requirements depend on the array design, and the tolerance on spacing can be as small as 5nm, so is could be challenging. However center lines spacing is usually the easiest dimension to control because it is directly related to the interferometer on the stage of the mask making tool or, when using electron beam direct-write) of the electron beam tool. The required defect densities also should be reachable. The area of the waveguide array is less than that of current IC's requiring more than 20 levels of patterned structure. Thus patterning a single layer waveguide array to meet the OPA requirements appears within the current state of the art although more analysis on the effects of dimensional imperfections is needed.

Making a multi-level structure such as that shown in Fig. 1 might well be more challenging. It is similar to the problems presently being faced by those developing 3-D integrated citcuitry in that we need multiple levels of features made in device-quality single crystal silicon or germanium and embedded in $SiO_2$. There are two scenarios. One in which there is active circuitry in the structure and one where there is not. The crucial difference is that in the former we are restricted to temperatures compatible with devices already in the assembly; this is usually about 400C. The ability to employ higher temperatures in the bonding of multiple layers allows greater choice in the materials and processes used. It may be necessary to employ some chemical mechanical polishing to assure sufficiently flat and planar surfaces. The other challenge, common to both scenarios, is the need to overlay accurately the different layers. If we have only a 10nm tolerance then the problem becomes very challenging. Even achieving 100nm tolerance between levels is only just being approached by some of the groups pursuing 3-D integrated circuitry. Thus here again we need more understanding of the required tolerances in layer-to-layer overlay as well as continued effort on achieving nanometer scale overlay precision.

We will present our approaches to address the above mention challenges and the results. A 2-D SOI-based beam steering systems and its performance evaluation will also be presented.

[1] P. McManamon, T. Dorschner, D. Corkum, L. Friedman, D. Hobbs, M. Holz, S. Liberman, H. Nguyen, D. Resler, R. Sharp, and E. Watson, "Optical phased array technology," Proceedings of the IEEE, vol. 84, no. 2, pp. 268–298, 1996.

[2] A. Hosseini, D. N. Kwong, and R. T. Chen, "Unequally Spaced Waveguide Arrays for Silicon Nanomembrane-Based Efficient Large Angle Optical Beam Steering," IEEE Journal of Selected Topics in Quantum Electronics, vol. 15, no. 5, 1439-1446, 2009.

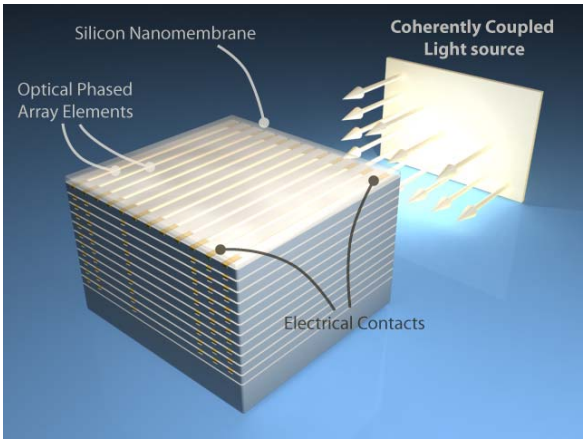


Fig. 1. A schematic of silicon nano-membrane-based OPA beam steering

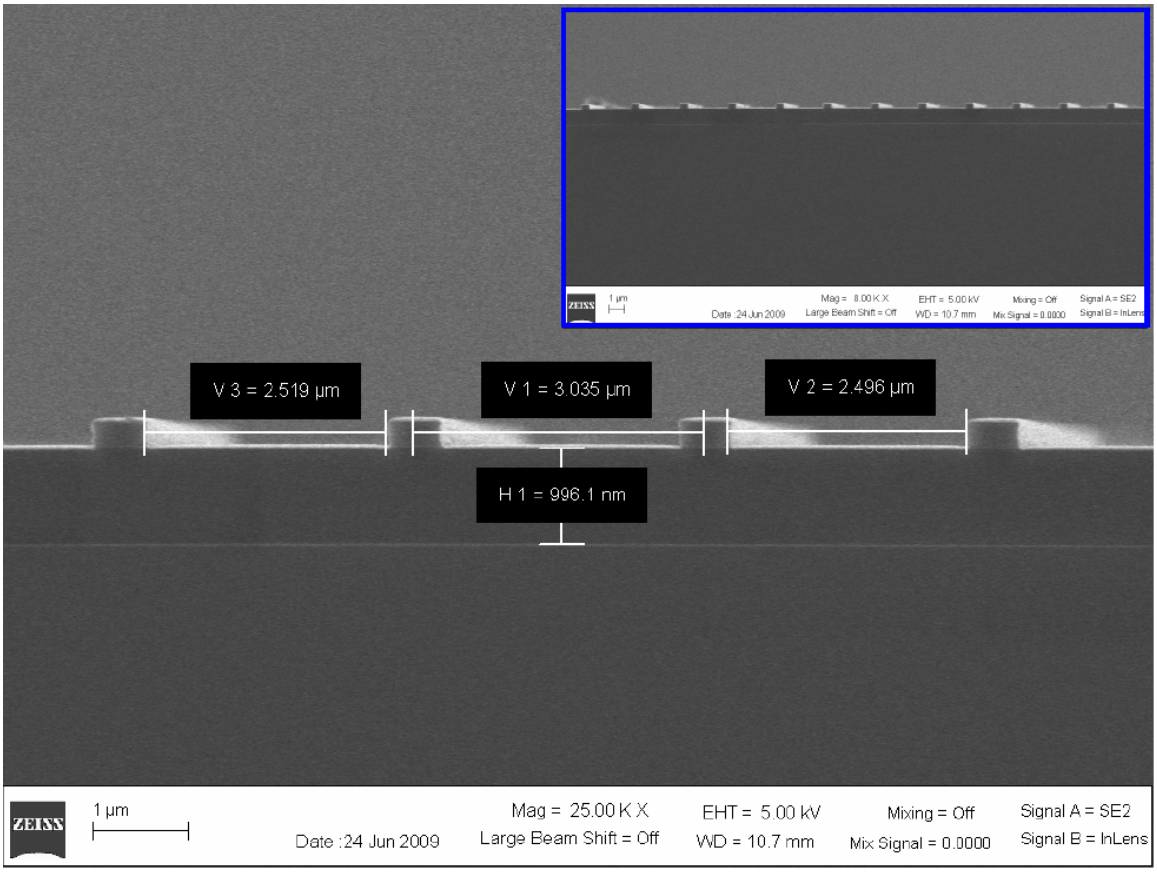


Fig. 2. Cross-section SEM picture of the fabricated 2D SOI-based OPA.