Silicon nanowires fabricated using FIB implanted Ga^+ etch masks for plasma etching

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As Moore's Law continues a drive to smaller scales, new top-down fabrication techniques will need to emerge to achieve nanoscale devices in silicon. This work demonstrates using a Focused Ion Beam (FIB) to implant Gallium ions (Ga^+) in silicon to act as a 20 nm thick etch mask for inductively coupled plasma reactive ion etching (ICP-RIE) of both vertical and horizontal nanowires down to 30 nm diameters, **fig 1** and **fig 2**. We demonstrate how these etch masks offer high selectivity for fluorinated mixed-mode etch chemistries including: anisotropic etches of SF_6/C_4F_8 (termed pseudo Bosch here) and Cryogenic silicon etches, as well as isotropic SF_6 etches. Pattern writing using a FIB permits silicon patterning with resolution near to that of electron beam lithography without requiring resist or any wet chemicals, so called dry-lithography. Further we demonstrate advantages of direct beam writing such as multilevel lithography, grayscale lithography, and a technique to pattern vertical sidewalls.

In order to achieve nanoscale devices, we experimentally determined the required critical areal doses required to achieve specific etch depths and structure sizes for both the pseudo Bosch silicon etch and the cryogenic silicon etch. We demonstrate, that unlike the cryogenic silicon etch, the linearity of the pseudo Bosch's 'critical dose - etch depth' curve enables precision grayscale lithography, **fig 3**. We intend on demonstrating a vertical blaze diffraction grating as an example of this technology.

Unlike photo or electron beam resist, FIB mask patterning does not require a planar silicon surface. This fact enables multilayer lithography in silicon; Ga^+ patterning, followed by a silicon etch, followed by a Ga^+ re-patterning, and concluded with a silicon etch. Since the implanted Ga^+ layer is resilient against fluorinated etch chemistries, we also demonstrate how the multiple etch steps are not required to use the same chemistry. Here we use the pseudo Bosch etch to define micron scale pillars, and then use the cryogenic etch to undercut a silicon nanowire positioned between the structures. The combination of the two etches permits fabrication of suspended silicon nanowires between the micropillars at various etch heights, **fig 4**.

Finally, we intend to demonstrate how to use the Ga^+ rich masking layer for electrical contacts to nanowires. After etching, we anneal the damaged silicon and activate the Ga^+ to create a P^+ surface layer ideal for ohmic contacting to nanowires. The I-V characteristics of the nanowire are then measured using an Agilent Semiconductor Parameter Analyzer.

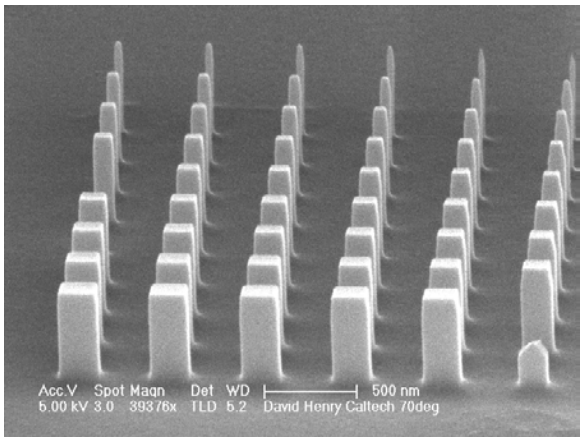

Fig 1. SEM of silicon square pillars 525 nm tall. The sizes start at 40nm and increase in 20nm increments to 200nm. The areal dose of the implanted Ga was varied in steps to establish the critical dose array for the Pseudo Bosch silicon etch.

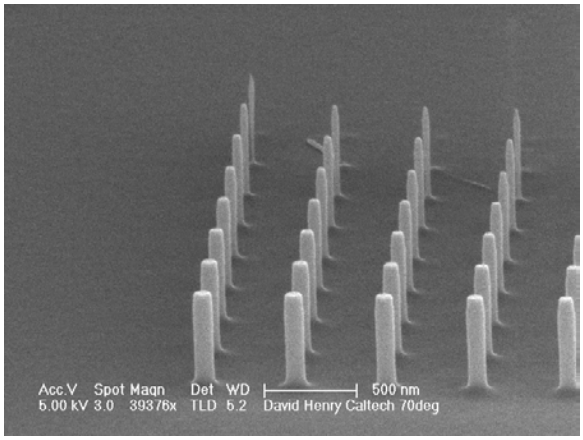

Fig 2. SEM of Ga^+ masked, etched silicon nanopillars. Etch depth using Pseudo Bosch chemistry was 448nm with the pillars ranging from 100nm down to 30nm diameters in 10nm increments.

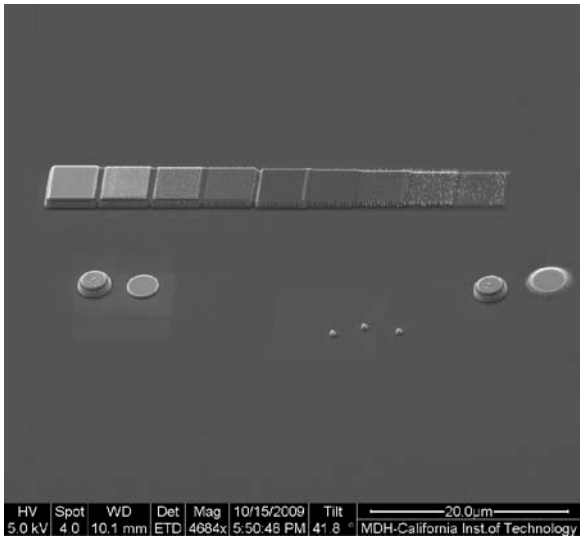

Fig 3. SEM of 5um x 5um squares in silicon masked with stepped areal doses of implanted Ga^+. Each square's height is determined by selecting the critical areal dose. This demonstrates that Grayscale lithography is achievable using Ga^+ implantation.

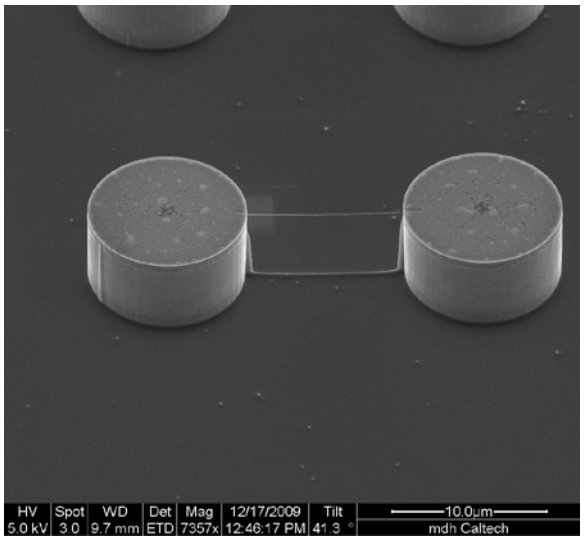

Fig 4. SEM of multilevel Ga^+ implantation lithography and etching in silicon to create a 80nm x 20nm wire, 10 microns long. The wire is suspended ½ micron below the surface. Two different silicon etch chemistries and implanted Ga^+ lithography steps were utilized to make the structure.