Novel Pulsed Spot Milling Technique to Extend Gallium Ion Beam Technology for Circuit Edit

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The opportunity for circuit edit success using any focused ion beam (FIB) system requires an analysis of via profiles (1) relative to the geometries required by a particular FAB process technology. Progressively smaller technology geometries demand a corresponding reduction in spot size (i.e. ion beam resolution). For example, process technologies beyond the 32nm technology node show a minimum critical line pitch trend < 100nm and an ion beam spot size requirement trend < 5nm (2). Advanced definitions of effective resolution include consideration of signal to noise ratio (2, 3) and discerning circuit edit technologists also demand high-performance beam rastering (Fig 1) to yield high-quality, small-geometry features based upon well-defined recipes that provide optimum chemistry-assisted process control and endpointing (2). This conceptual model is adequate for limiting an invasive impact to lateral features (perpendicular to the incident beam) but does not account for damage that could occur as a result of unintended penetration to processing layers directly below the targeted interconnect region (Fig 2).

Decreasing the beam energy generally results in an increase in spot size (4), therefore users and tool developers tend to maintain relatively high beam energy levels. High beam energy tends to result in unintended over-etch or etching during intended depositions (Fig 4). Forward damage approaching the active regions of a transistor may also occur and can dramatically change device performance (5). Spot-size and rastering are certainly important FIB processing attributes; however, greater emphasis must be placed upon depth penetration and must be added as a key factor in the definition for acceptable engineering criterion at the smallest possible geometries.

To enable circuit edit work for geometries required by the 22nm technology node, a new technique has been employed, pulsed spot milling (PSM). PSM eliminates the need for beam rastering which is substituted by a single-point ion beam of process-matched energy (Fig 3) and a modulated dwell time. PSM is enabled by a new ion column design and novel chemistry-assisted processes to yield high-quality, predictable, reliable and repeatable vias <50nm diameter that are both laterally and vertically robust with minimal dependency on visual endpointing. The implementation of these new operational principles and ion control hardware on a stable and reliable gallium ion platform yields success for existing process technologies and shows a clear path to intercept 22nm technology nodes and beyond.

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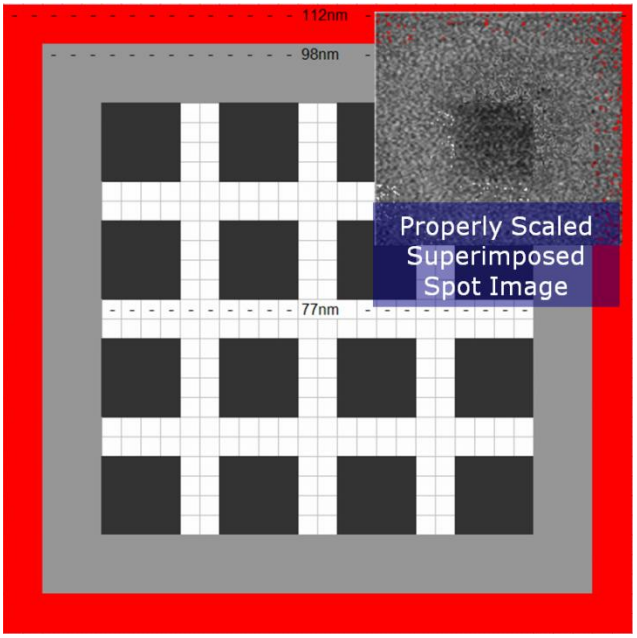

Figure 1 – Typical FIB spot shape and rastering plan for a 100nm diameter via. The diagram represents a properly scaled via plan with a superimposed spot using legacy tools and processes. The individual interior squares represent a practical spot size of 14nm positioned in evenly-spaced raster intervals. The borders represent unintended via profile expansion. The interior border represents ion beam tails and the outer border represents the effect of typical beam deflection errors. Spot size, beam tails and deflection errors combine to create the overall mill geometries and must be considered when rastering.

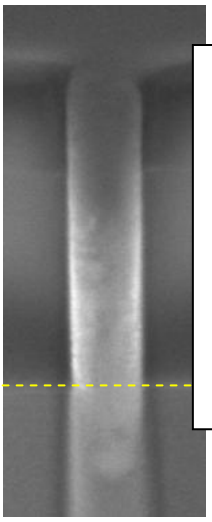

Figure 2 – High quality, high aspect ratio FIB via showing excessive depth penetration Users and tool developers tend to maintain high beam energy levels that cause unintended depth penetration during via formation. (110nm diameter via produced at 30kV shown).

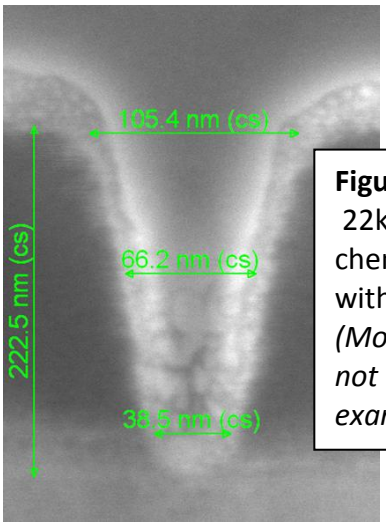

Figure 3 – Spot Mill Via 22kV 2pA XeF_2 chemistry-assisted etch with $Mo(CO)_6$ back-fill. *(Modulated dwell time not employed in this example.)*

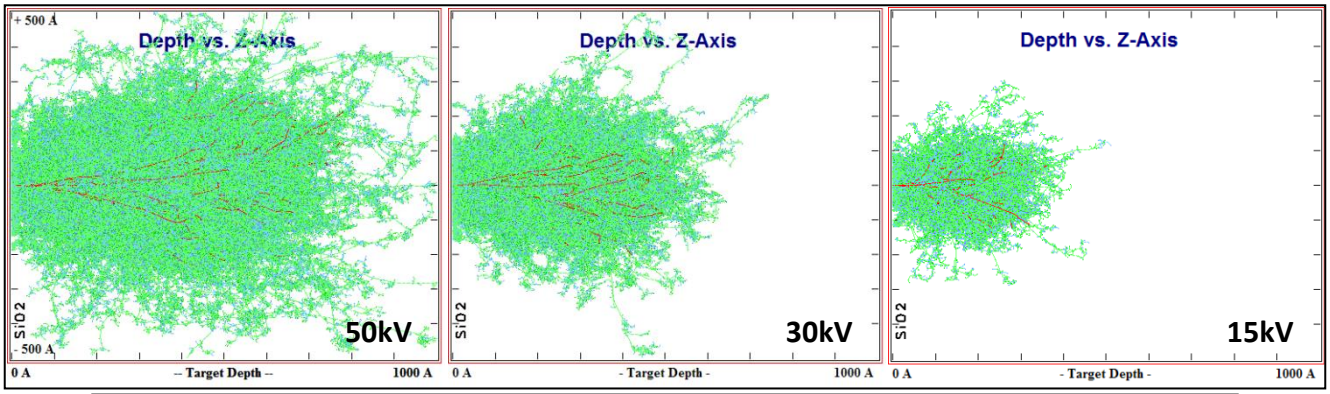

Figure 4 – Ion Beam Penetration and Collision Events for Various Beam Energies (6) *SRIM modeling shows beam penetration and collision events are minimized by lower accelerating voltages.*