Graphene Nanomeshes with Sub-10 nm Ribbon Width Fabricated via Nanoimprint Lithography in Combination with Block Copolymer Self-Assembly

Xiaogan Liang,[1,*] Yeon-Sik Jung[1], Shiwei Wu[1], Ariel Ismach[2], Deirdre L. Olynick[1], Stefano Cabrini[1], and Jeffrey Bokor[1,2]

[1]Molecular Foundry, Lawrence Berkeley National Laboratory, 1 Cyclotron Road, Berkeley, CA 94720

[2]EECS Department, University of California, Berkeley, CA 94720

Graphene is of great interest not only as a superior electronic material but also as a promising platform for the investigation of new mesoscopic phenomena.[1] Recent experimental work has shown that graphene nanoribbons (GNRs),[2] quantum dots (QDs),[3] and heterojunctions,[4] incorporated into nanoelectronic structures, exhibit different transport behavior than conventional semiconductor quantum devices (for example chaotic Dirac Billiard in Coulomb blockade,[3] Klein tunneling,[4] and anomalous Hall effects[5]). Recent theoretical work predicts more novel and counter-intuitive properties for nanoscopic graphene structures, such as strong conduction anisotropy and subband formation in graphene superlattices.[6] In order to fabricate the appropriate nanoscopic graphene structures, novel nanopatterning routes are needed. These nanopatterning techniques require nanoscale periodic or quasi-periodic modulations (e.g. selectively etched meshes, doped areas, or topographically-induced strain). In addition, patterning over large areas is necessary for producing functional arrays of graphene nanostructures (e.g. GNRs) over wafer-sized areas.

In this work, we fabricated hexagonal graphene nanomeshes (GNMs) with sub-10 nm ribbon width. The fabrication combines nanoimprint lithography,[7] block-copolymer self-assembly for high resolution nanoimprint template patterning,[8] and multiple techniques for graphene deposition (electrostatic or mechanical exfoliation).[1, 9, 10] Graphene field-effect transistors (GFETs) made from GNMs exhibit very different electronic characteristics in comparison with unpatterned GFETs even at room temperature. We observe multi-plateaus in the drain-source current (I_{ds}) – gate voltage (V_g) dependance as well as an enhancement of I_{ON}/I_{OFF} with shrinking ribbon width of GNMs. These effects are attributed to the formation of electronic subbands in GNMs.

Figure 1 shows the nanoimprint process used to fabricate the graphene hexagonal mesh with 10 nm and below graphene ribbon widths. The hexagonal imprint template was fabricated using a self-assembled diblock copolymer mask to etch the pattern into an SiO2 template blank.[8] Figure 2 shows the I_{ds}-V_g characteristics of a GNM-based GFET at room temperature. Persistent multi-plateaus in the I_{ds}-V_g curves are observed for various V_{ds}, which is an important sign for the formation of subbands in the electronic structure of graphene nanomeshes.[2] Additional analysis of the effect of GNM geometries on I_{ON}/I_{OFF} ratio will be presented. This work shows that nanoimprint lithography is a pathway for low-cost, high-throughput production of mesoscopic graphene structures with critical dimensions down to single-digit nanometer regime, and is compatible with wafer-scale applications.

This work was supported by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231.

[1] A. K. Geim andK. S. Novoselov, Nature Materials **6**, 183 (2007)
[2] M. Han, B. Ozyilmaz, Y. Zhang, and P. Kim, Phys. Rev. Lett. **98**, 206805 (2007)
[3] L. Ponomarenko, F. Schedin, M. Katsnelson, R. Yang, E. Hill, K. Novoselov, A. Geim, Science **320**, 356 (2008)
[4] A. Young and P. Kim, Nature Physics **5**,222 (2009)
[5] V. Gusynin1 and S. Sharapov, Phys. Rev. Lett. **95**, 146801 (2005)
[6] C. Park, L. Yang, Y. Son, M. Cohen, and S. Louie, Nature Physics **4**, 213 (2008)
[7] S. Chou, P. Krauss, and P. Renstrom J. Appl. Phys. Lett. **67**, 3114 (1995)
[8] I. Bita, J. Yang, Y. Jung, C. Ross, E. Thomas, K. Berggren, Science **321**, 939 (2008)
[9] X. Liang, Z. Fu, S. Chou, Nano Letters 2007, 7, (12), 3840-3844
[10] X. Liang, A. Chang, Y. Zhang, B. Harteneck, H. Choo, D. Olynick, and S. Cabrini Nano Lett. **9(1)**, 467-472 (2009)

* Email: xliang@lbl.gov

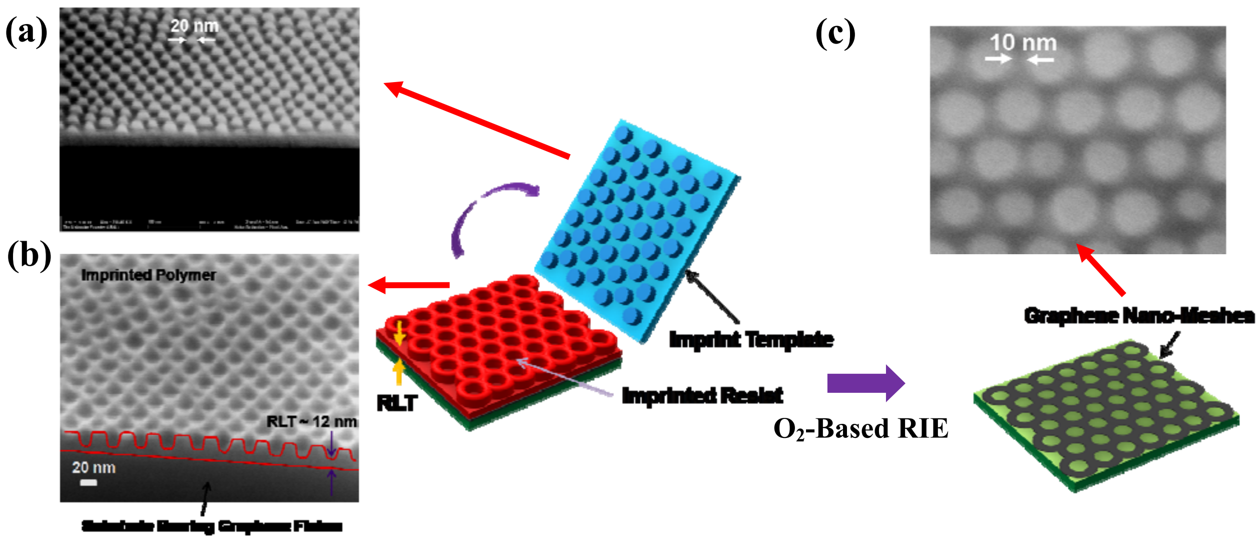

Fig. 1 Graphene nanomeshes (GNMs) fabricated via nanoimprint lithography. SEM images of (a) a silicon nanoimprint template bearing hexagonally-arranged 20 nm dia. posts. Structure was fabricated using a block-copolymer self-assembled mask and RIE (well-ordered periodic domain size ~ 100s nm); (b) thermally imprinted resist on top of a graphene film, and (c) GNMs with 10 nm wide ribbon after etching through the imprinted resist residual layer (RLT) and the underlying graphene (1- or 2-LGs) followed by resist removal.

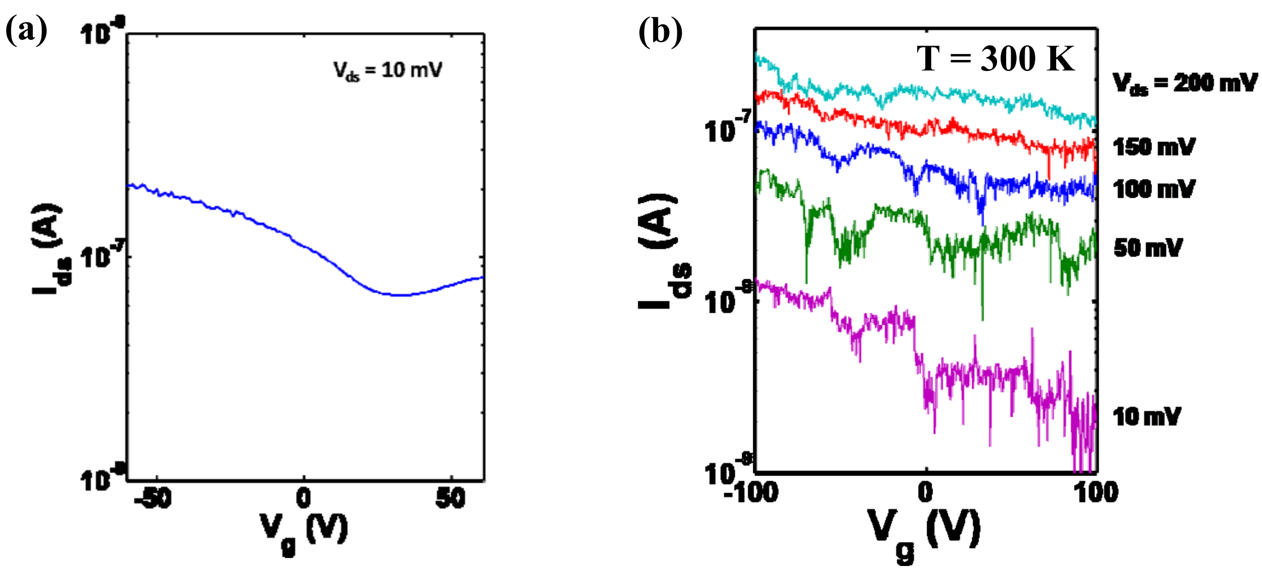

Fig. 2 $I_{ds} - V_g$ curves of (a) unpatterned GFET and (b) a GNM GFET (2-LG) for various values of V_{ds} measured at room temperature. The device has an average GNM ribbon-linewidth of 10 nm; total channel length and width of 2 and 1.4 μm, respectively. Cr/Au was deposited as metallic drain and source. The GNM FET exhibits distinctive $I_{ds} - V_g$ characteristics compared to unpatterned graphene FET. Multi-plateaus are found and remain persistent at various V_{ds}, indicating the formation of subbands in the electronic structure even at room temperature.

* Email: xliang@lbl.gov