Nanoscale 2- and 3-Terminal Resistive Switching Devices

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Transition metal oxide based resistive switching devices (memristors) are promising candidates for the next generation non-volatile random access memory (NV-RAM) and neuromorphic networks [1, 2]. Here we present TiO_2 based lateral resistive switching devices with sub-3 nm feature size that were fabricated using nanoimprint lithography (NIL) [3] and angle evaporation. These devices have reliable bipolar switching behavior with up to 10^3 ON/OFF conductance ratios. Furthermore, we demonstrate that the resistance of the TiO_2 can be modulated electrically by a third electrode, implementing a nanoscale memistor device function.

In fabrication, a 50 nm wide, 12 nm thick (3 nm Ti/9 nm Pt) nanowire was first made on a flat substrate (100 nm thick thermally grown SiO_2 on Si) using NIL, reactive ion etching (RIE), metal evaporation and liftoff (Fig. 1a). A thin layer of switching material (e.g., 28 nm thick TiO_2) was then deposited on the sample using a DC sputtering system. The height of the nanowire on the substrate created a protrusion in the switching layer (Fig. 1b). A second set of NIL, RIE, metallization and liftoff processes were carried out to make the top wires (50 nm wide, 15 nm thick Pt) orthogonal to the bottom ones on the TiO_2 layer. The top metal wires were deposited with an oblique angle to the substrate surface. Due to shadow effect from the protrusion, this deposition created two segments separated by a gap for each wire (Fig. 1c).

Fig. 2 shows scanning electron microscope (SEM) images of the devices with different gap sizes. With a 75° evaporation angle, the lateral distance between the two segments of wire was 2.8 nm (Figs. 2a, b). Decreasing the angle to 45° resulted in a gap size of 5 nm (Figs. 2c, d). Further reducing the evaporation angle to 30° and 15° led to gap sizes of 10 and 50 nm, respectively (Fig. 2e, 2f).

To test the electrical behavior, we applied a voltage across the gap by contacting both segments of the top wire. The current-voltage plots in Fig. 3 give typical switching curves for 10, 5 and 3 nm gap devices. The switching ratio of all the lateral devices was greater than 100 (up to 1000 for the 5 nm device). The devices were still switchable after 100 cycles.

To operate the devices in the 3-terminal mode, we applied a voltage (V_B) to the bottom electrode to modulate the resistance of TiO_2 between the two top electrodes (Fig. 4a). The resistance was then measured with a much lower voltage (V_{ts}) after removing V_B. The device was switched ON and OFF reliably (Fig. 4b), and repeatable resistance modulation with a factor >20 was achieved (Fig. 4c). This demonstrates the memistor behavior as proposed by Widrow [4] but with a much smaller device.

Our work demonstrates that the switching physics works even at sub-3 nm regime for resistive switching devices (memristors and memistors). The modulation of the resistance in the switching materials will enable a wider control over the device properties, and find applications in the fields such as NVRAM and artificial neural networks.

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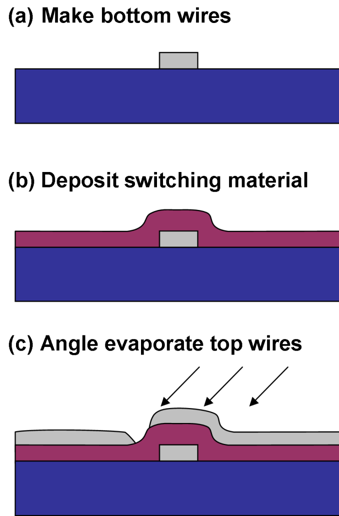

Fig. 1. Schematics of the fabrication principle. (a) A bottom wire is made on a flat surface. (b) After depositing a thin layer of switching material, a protrusion is created on the surface. (c) The top wires are patterned and deposited with an angle to the surface, leaving a gap in between the two segments.

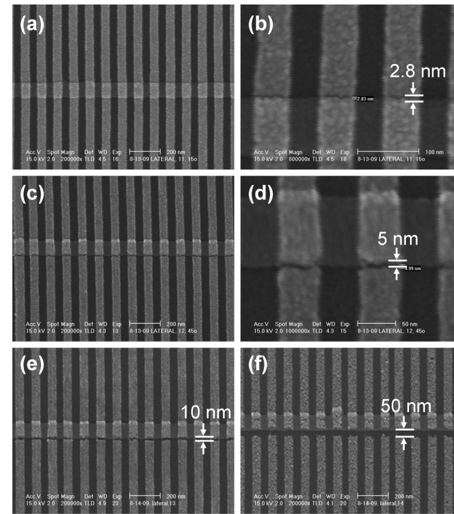

Fig. 2. SEM images of the lateral devices with different gap sizes. (a) 75 ^{o}, 2.8 nm gap size. (b) Zoom in image of (a). (c) 45 ^{o}, 5 nm gap size. (d) Zoom in image of (c). Evaporation angles of 30 ^{o} (e) and 15 ^{o} (f) give gap sizes of 10 nm and 50 nm, respectively.

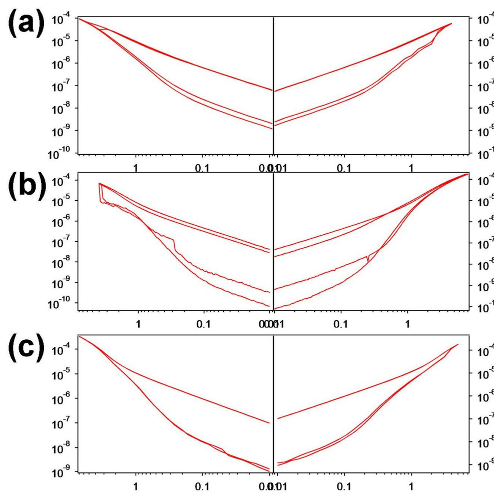

Fig. 3. Switching behavior for lateral memristive devices with (a) 10 nm (b) 5 nm and (c) 3 nm gap sizes (the first 2 cycles shown here). The data are plotted in a log-log scheme (Horizontal: V; Vertical: A). All the devices exhibit bipolar non-volatile switching behaviors.

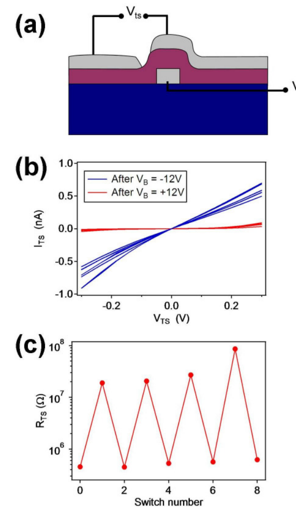

Fig. 4. Demonstration of a memistor behavior. (a) The measurement for the 3-terminal device. (b) The resistance of the ON (blue) and OFF (red) states. (c) Plot of device resistance as a function of cycle numbers. The device used in this study has a feature size of 3 nm.