Novel lateral size reduction technique to fabricate sub-12 nm Si integrated circuits

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While extensive research is currently being pursued for various next generation lithographic (NGL) techniques (*e.g.* Extreme Ultraviolet (EUV), Electron Beam and Focused Ion Beam, and Nano-imprinting), this paper presents a novel approach which reduces feature size beyond mask-determined dimensions and potentially provides ~1nm line edge roughness (LER). The methodology is generic and is applicable to any lithographic technique. It is specially suited in the formation of sub-12nm n-channels of FETs. The methodology involves: (a) forming a pattern (channel/gate) with a given lithographic method (e.g. EUV), (b) laterally reducing the p-region size by extending the adjacent n-type regions via rapid thermal annealing of ultra-shallow implants (forming the source and drain), and (c) site-specifically self-assembling of cladded SiO_x-Si or GeO_x-Ge quantum dots (2-6nm) which deposits only on p-doped regions. The small dot diameter ensures the desired LER.

Reduced lateral size reduction via Ultra-low Energy (ULE) Implants, Rapid Thermal Anneal, and Site-Specific Self-assembly of SiO_x-Si nanoparticles: In this approach, we start with relatively larger patterns (*e.g.* in SiO_2 layer on Si substrates) using a conventional lithographic method. This is followed by reduction of the lateral pattern size by a factor of 2-4 (with LER limited by the size of self-assembled nanoparticles). For example, we have achieved 30 nm x 30 nm patterns by reducing 60 nm x 60 nm patterns (pink squares in Fig. 1, which are created by employing E-Beam lithography) via a processing technique that creates SiO_x nanopatterns/nanomasks using site-specific self-assembly of SiO_x-on-Si nanoparticles in predetermined regions. Reduction of 30 nm features to sub-12 nm is in progress (in collaboration with ASML researchers).

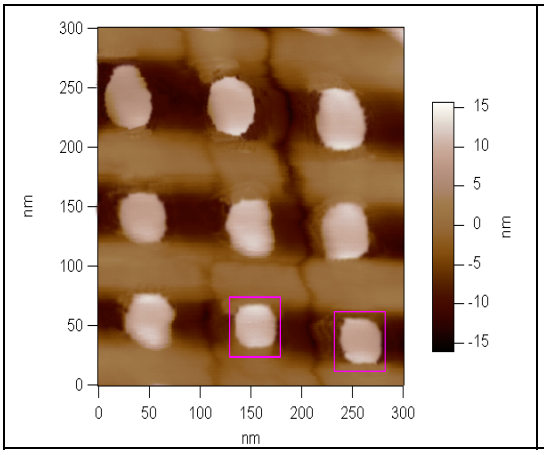

Fig. 1. Scanning electron micrograph of 30-35nm nano-island array formed using site-specific self-assembly of SiOx-Si nanodots (~6 nm).

The *lateral size reduction* of a given pattern depends on: *(1)* the precision with which regions are doped, by combining ultra-low energy (ULE) shallow ion implants (14-50 nm) followed by rapid thermal annealing, and *(2)* resolution of the site-specific self-assembled SiO_x-Si nanoparticle layer [e.g. size (3-8 nm) of nanoparticles and the layer thickness (number of assembled layers). The concept is shown schematically in Fig. 2.

Figure 2(a) shows schematically the reduction of starting 100 nm x100 nm patterns to 30 nm x 30 nm patterns by shallow n-implants and lateral diffusion during rapid thermal anneal (RTA). This is followed by site specific self-assembly on reduced p-regions [green squares in Fig. 2(b)]

after the SiO_2 layer is removed. The present approach reduces the channel length/Width in FETs below mask-features, thus permitting increasing the overall packing density.

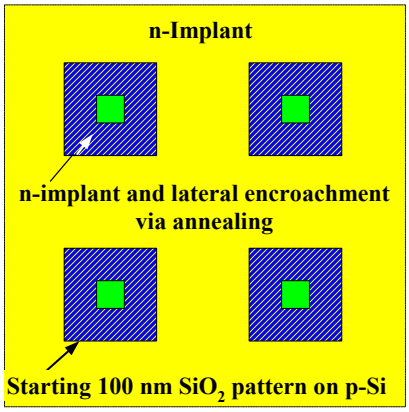

Fig. 2(a) left. 100 nm squares (blue) of patterned SiO_2 showing lateral diffusion on n-dopants (shaded) on p-Si (yellow),

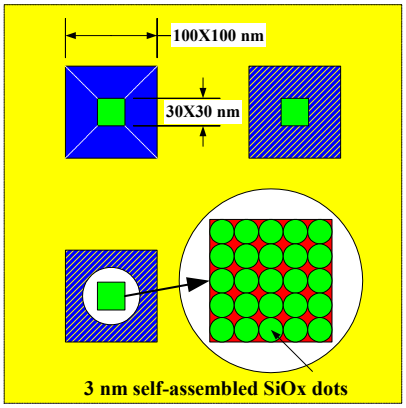

Fig. 2(b) 30 nm squares (green) with self-assembled 3nm SiOx-Si dots (after removing original SiO_2 (blue).

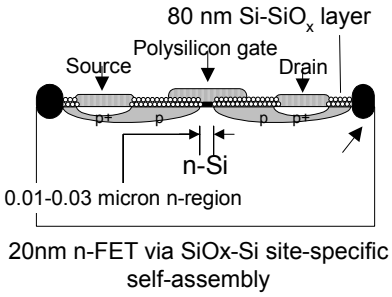

Fig. 3 SiO_x-Si nanoparticle self-assembled on p-regions to realize a 10-30 nm n-Si FET [15].

Sub-12nm FETs: There has been a significant effort over the past decade to fabricate Si/SiGe scaled-down CMOSFETs with 12 nm SiGe [1] and double gate FinFETs [2]. Fabrication of integrated circuits using scaled down FETs requires significant improvements in lithography [3, 4], shallow implants, and site-specific self-assembly of SiO_x-Si nanoparticles [5]. Fig. 3 shows schematically an n-channel ~ 10 nm gate FET involving site-specific self-assembly and lateral size reduction methodology integrated with other processing steps.

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