Semiconductor Crystal Islands for 3-Dimensional Integration

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The critical operation needed to achieve 3-dimensional integrated circuits[1] is obtaining single-crystal, device-quality semiconductor material on upper circuit layers without damaging circuits below (400°C temperature limit). Simulations suggested that microsecond pulse 532nm Nd:YAG laser could melt and crystallize amorphous Si or Ge layers without heating the circuit layers underneath[2]. However, experimental results of unseeded (graphoepitaxy)[3] and seeded (RMG) crystallization of Si and Ge indicated that much longer pulse lengths are required for high quality single crystal formation, rendering the approach not 3DIC compatible.

A more straightforward approach is to directly attach high quality crystal islands for upper layer device fabrication. The authors identified and investigated a variety of viable low-temperature (≤400°C) bonding methods: fusion bonding (SiO_2-SiO_2, Si-SiO_2, Ge-SiO_2), thermo-compressive bonding (Cu-Cu, Ti-Ti), as well as AlGe eutectic bonding.

Here we report our experiments demonstrating successful attachment of both silicon and germanium crystal islands onto amorphous SiO_2 substrates using hydrophilic fusion bonding at 400°C. Prime Si (100) wafers and Ge (100) epi wafers were first patterned into islands (2um – 3000um in size) to serve as donors (Fig. 1). Oxidized (SiO_2) acceptor wafer was placed together with the donor wafer into NH_4OH:H_2O_2:H_2O (5:1:1) solution at 70°C to chemically activate the surfaces. Upon room temperature fusion bonding, samples were annealed at 400°C to strengthen the bond and eliminate interfacial voids. The island structure proved advantageous in out-diffusion of interfacial gas byproducts, thus greatly reducing the occurrence of thermally induced voids. With hydrogen induced splitting (SmartCut™) of the donor wafer, the transfer of crystalline islands onto SiO_2 substrate was complete (Fig. 2). Finally, the remaining island surface roughness was removed using CMP touch polish (Fig. 3 and 4).

In an effort to realize upper layer devices of a monolithic 3DIC, a low-temperature (≤400°C) process was developed to fabricate PtSi Schottky source/drain MOSFET (Fig. 5). Experiments are underway to utilize this process to fabricate monolithic 3DIC devices on the attached Si (100) islands.

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[2] D. Witte et al., *Microelectronic Engineering*. **84** (2007) p.1186.
[3] F. Crnogorac et al., *Journal of Vacuum Science and Technology B*, 26 (2008), p. 2520-2523.

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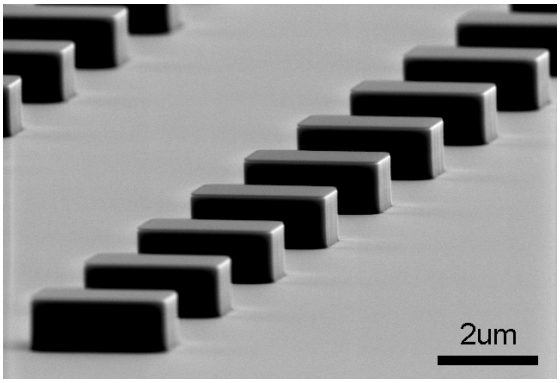

Fig 1. Donor prime Si (100) wafer with patterned islands ready to be transferred.

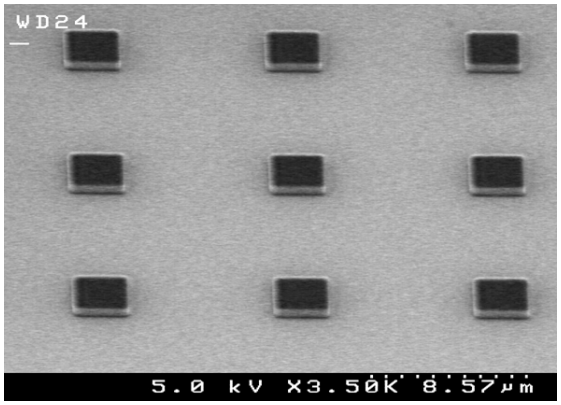

Fig 2. Resulting array of Si (100) crystal islands (400nm high) on top of SiO_2 acceptor substrate.

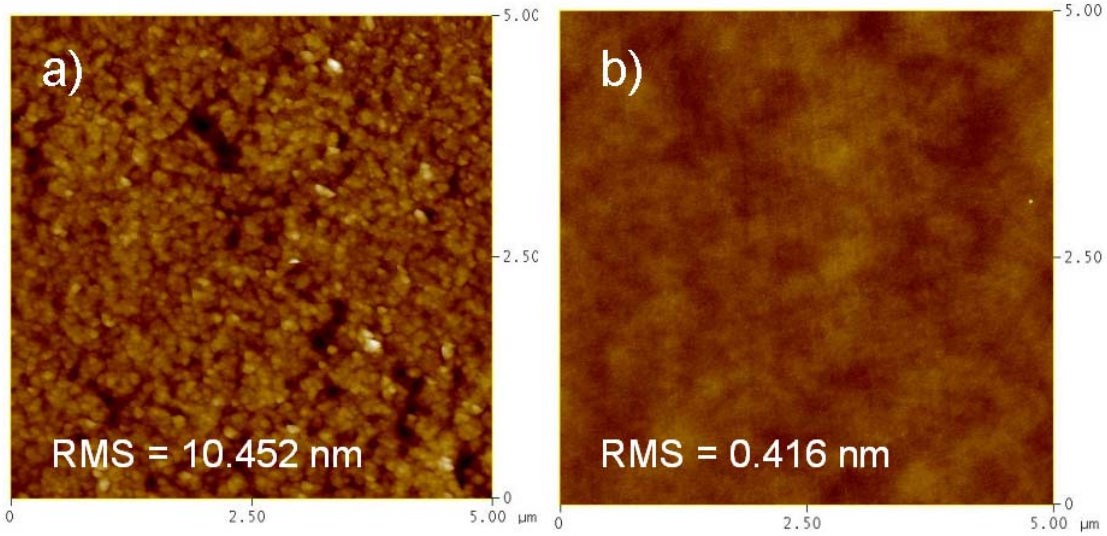

Fig 3. AFM scan (5µm x 5µm) of silicon island surface roughness: a) post SmartCut, and b) after touch polish (CMP) with colloidal silica based slurry.

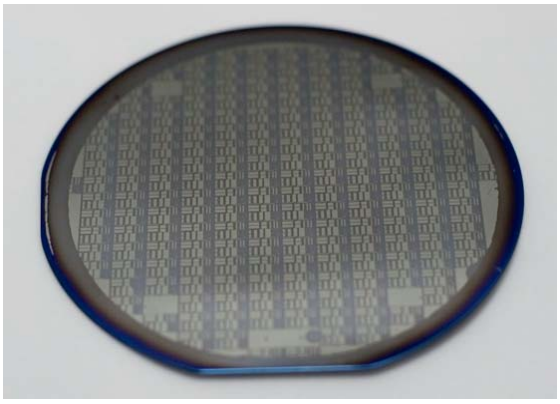

Fig 4. Post-CMP 4" acceptor wafer with Ge (100) crystal islands on top of SiO_2.

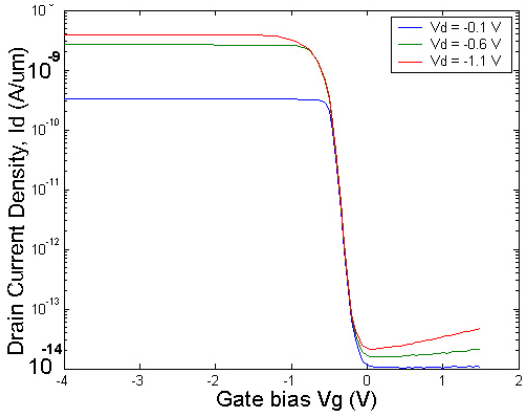

Fig 5. I_D-V_G characteristics of low-temperature (≤400°C) processed PtSi Schottky source/drain MOSFET on bulk Si (100).