A 1D Gridded Design Style for Hybrid Optical and e-Beam Patterning

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Semiconductor patterning was facing a crisis in the early 2000's as many "red bricks" were appearing in the ITRS. Fortunately, immersion lithography was commercialized and in production for the 45nm CMOS logic node.[1] A path to 7nm CMOS using hybrid patterning was recently described, with some issues noted for nodes beyond 16nm.[2] The concept of using optical lithography, either with masks or interferometers, for "lines" combined with e-beams for "cuts" has been discussed for several years.[3,4]

Conventional logic design has used 2D patterns with bends and other non-rectangular shapes. A different design style, using 1D gridded features, has been developed to enable effective use of HOMA (Hybrid Optical MAskless lithography) techniques.[5] Figure 1 shows a comparison between 2D conventional and 1D gridded design styles.

Figure 2 shows why the issue of design style and the use of HOMA is of current interest. The "A" scaling path will require pitch-division-by-2 (PD2) at 22nm, while the "B" path will require PD2 at 16nm. In either case, the "cut" pattern will be extremely challenging for metal-1 at 16nm.[6]

An example metal-1 pattern using lines and optical cuts is shown in Figure 3 for 22nm "A" design rules with a 70nm pitch. The simulated optical cut pattern is merged with the lines to show the expected results after patterning. The SEM image shows the Damascene trenches in photoresist.[7] (Photo courtesy of Applied Materials.)

A serious problem for 1D gridded design of SOCs (System on Chip) is the current approach of designing logic cells and SRAMs with different styles. For example, typical SRAMs have the gate and metal-1 lines parallel, while the standard cells have these layers in perpendicular directions. The alternative is to design the logic and SRAMs to be unified from the beginning. In this case, critical layer orientations as well as pitches can be matched.[8]

Figure 4a and 4b show example layouts of logic cells and SRAM arrays, respectively. The gates are all aligned, on the same pitch. The metal-1 pattern, not shown, runs horizontally in both layouts, also on the same pitch. This unified design approach is required to support a 1D gridded design style implemented with lines and cuts.

Implications of HOMA lithography for SOC designs will be discussed. Maskless approaches for the line patterns, including interferometers and spacer double patterning, will be illustrated. The limitations of optical lithography for the cut and hole patterns will be presented, along with a discussion of current efforts in direct write e-beam lithography with emphasis on multiple beam approaches.

Keywords: gridded design rules, hybrid patterning, multiple e-beam lithography, interferometric lithography

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FIGURES

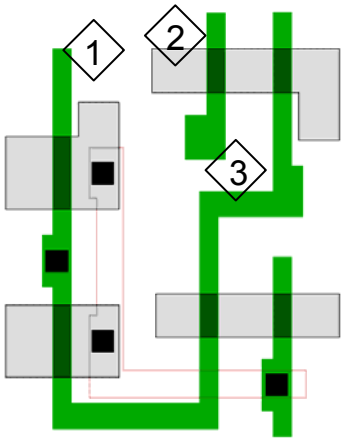

Figure 1a. Conventional 2D logic design style with problem areas: 1) isolated line, 2) semi-isolated line, 3) 2D bends and corners.

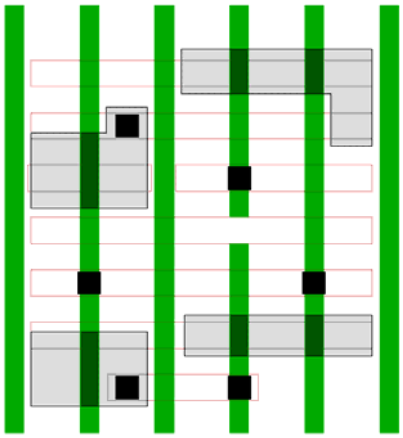

Figure 1b. 1D gridded design for CMOS logic.

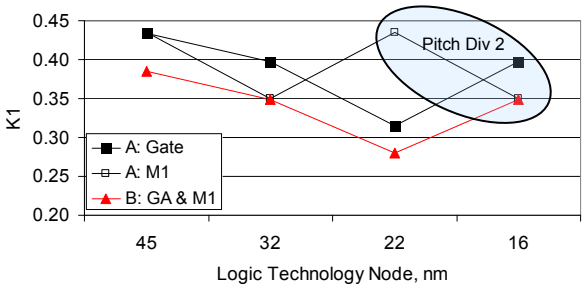

Figure 2. k1 trend for CMOS logic, with the transition to pitch division at 22nm / 16nm.

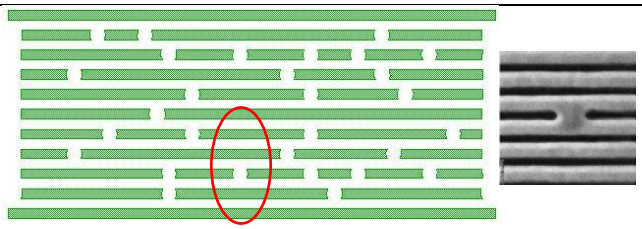

Figure 3. Metal-1 pattern for "A" design rules; simulated optical cut pattern and SEM of Damascene trenches.

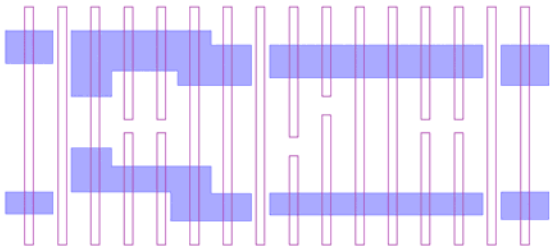

Fig.4a. Standard cell Active and Gate layers.

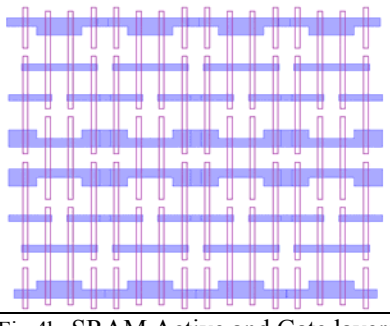

Fig.4b. SRAM Active and Gate layers.