Wafer level critical dimension control in spacer defined double patterning for sub-72 nm pitch logic technology

Ryoung-han Kim[1], Youri van Dommelen[2], Robert Watso[2], Jo Finders[2], Matthew E. Colburn[3], Harry J. Levinson[4]

[1]GLOBALFOUNDRIES, Albany, NY, [2]ASML, Albany, NY, [3]IBM Research, Albany, NY, [4]GLOBALFOUNDRIES, Sunnyvale, CA

Two double patterning techniques are currently under evaluation for logic applications in semiconductor industry [1]. Sidewall spacer double patterning is the technique that has been evaluated in memory manufacturing due to its advantage in self-aligning and highly unidirectional nature [2], and extends its era into the logic applications recently. Process demonstrations of uniform and controllable spacer deposition and etch into a pitch split pattern have been reported previously, however, it is not well known that variation in critical dimension (CD) of the core mandrel can give rise to an effective overlay shift to the layout circuitry, and therefore the CD uniformity control of the core mandrel at a wafer level is critical to implement the technology into the manufacturing.

In this paper, we will show that the CD uniformity driven effective overlay defines a new lithographic process window in the sidewall spacer double patterning, and provide a theoretical and empirical basis of the contribution to the CD uniformity variation in aerial image, chip-level and wafer-level printed image. Finally, effective methods of suppressing the CD variation using illumination optimization and active dose control across the wafer using ASML Spacer Controller™ are explored.

Keywords: Double patterning, Spacer, Critical dimension uniformity, Double Patterning, Self-align, Overlay, Controller

Reference:

[1] J. Finders, M. Dusa, B. Vleeming, H. Megens, B. Hepp, M. Maenhoudt, S. Cheng, and T. Vandeweyer, "Double patterning for 32nm and below: an update," Proc. SPIE, Vol. 6924, 692408 (2008)

[2] W. Jung, C. Kim, J. Eom, S. Cho, S. Jeon, J. Kim, J. Moon, B. Lee, and S. Park, "Patterning with spacer for expanding the resolution limit of current lithography tool," Proc. SPIE, Vol. 6520, 65201C (2007)

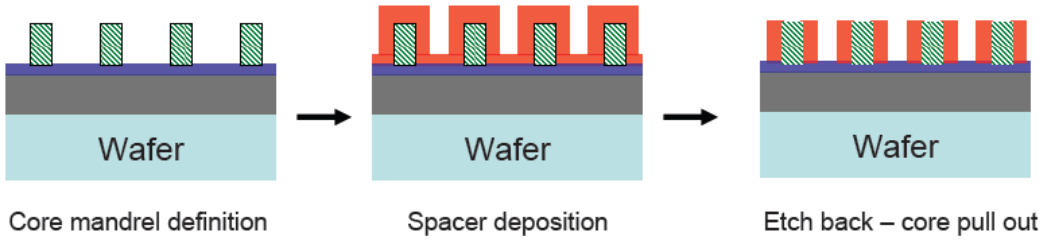

Fig. 1. Simplified process schematic of spacer pitch split

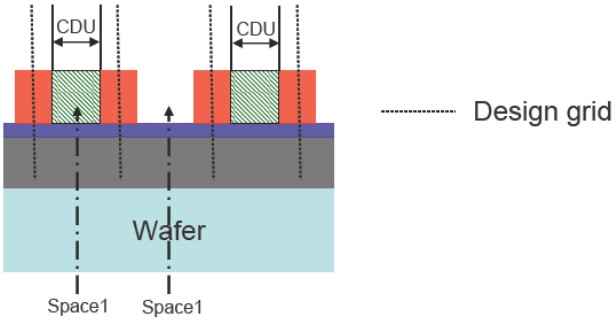

Fig. 2. Schematic illustration of spacer displacement due to core mandrel CD uniformity

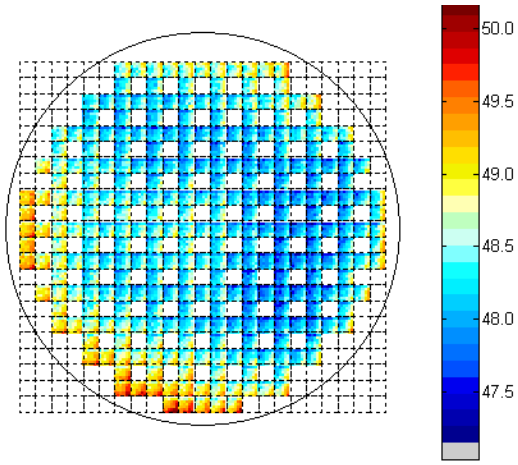

Fig. 3. Core mandrel CD finger print across the wafer before controller correction (CDU 3σ = 2.5 nm)

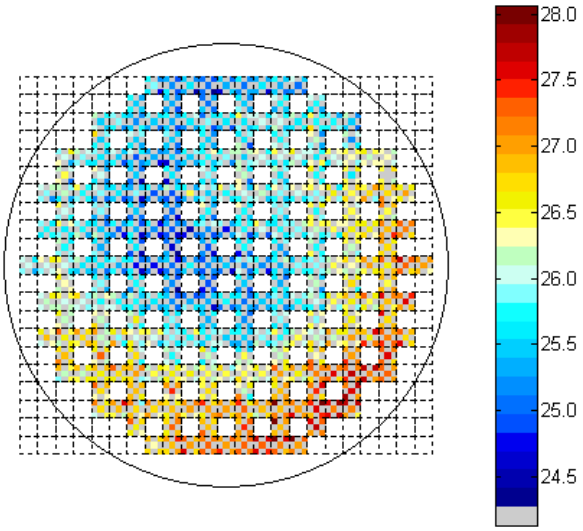

Fig. 4. Post etch space 1 CD finger print across the wafer before controller correction (CDU 3σ = 2.16 nm)

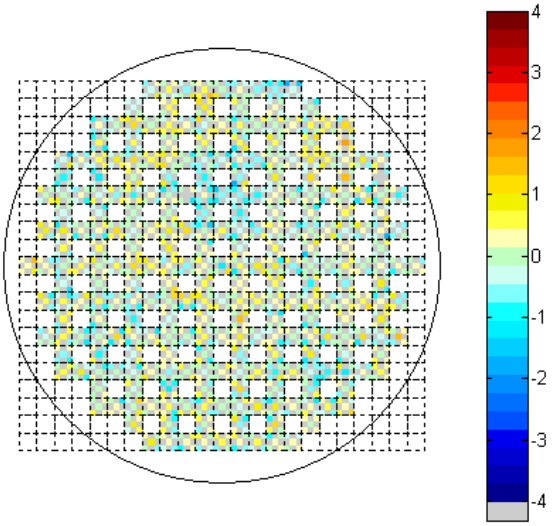

Fig. 5. Simulated post etch space 1 CD finger print across the wafer after controller correction (CDU 3σ = 2.16 nm) ; experimental data to be replaced