

Fabrication of platinum Single-Electron Transistors with Tunnel barriers made by Atomic Layer Deposition

*Hubert C. George, Alexei O. Orlov, Gregory L. Snider
Department of Electrical Engineering, University of Notre Dame, Notre Dame,
Indiana 46556*

We present a novel method for the fabrication of metal-oxide Single-Electron Transistors (SETs). The key feature of this SET fabrication method is the use of high quality insulating barriers produced by atomic layer deposition (ALD). Traditionally, metal-oxide SET fabrication methods use native metal oxides (TiO_2 , AlO_x , SiO_2) as tunnel barrier dielectrics. The restriction to materials with high-quality native oxides with reasonable material and growth properties significantly limits the choice of materials for SET fabrication. The use of ALD deposited barriers not only increases the number of material choices for SET fabrication but also allows atomic layer precision for tunnel barrier formation.

The fabrication method uses two electron beam exposure/metal deposition steps separated by a barrier dielectric deposition. Devices are fabricated on oxidized Si substrate. The first step is used to define the Pt leads (Source/Drain) of the SET, followed by the ALD deposition of 1 nm thick alumina (Al_2O_3) to create the tunnel barriers. Finally, the island of the SET is defined by a second e-beam exposure and Pt deposition.

Figure 1(a) shows an SEM micrograph of the SET after fabrication. Figures 1(b) and (c) show the I - V_{ds} and I - V_g characteristics of the device, in which we can clearly see a well developed Coulomb Blockade region and Coulomb blockade oscillations, respectively. Figure 2 shows the charging diagram of the SET, taken at 0.3K. From this diagram, we can observe three consecutive Coulomb diamonds and estimate the charging energy (E_C) to be 300 μeV . The moderate value of charging energy results from the relatively large capacitances of the junctions formed at the intersections of two metal wires (Fig 1(a)). We are currently optimizing the fabrication process to produce devices with higher charging energies by reducing the size of tunnel junctions and the SET's island. In addition, characterization of atomically deposited oxides is needed to achieve high quality and well controlled tunnel barriers.

Ultimately, this technique is targeted towards large scale production of SETs with atomically precise control of barrier fabrication that will speed up the adoption of SETs into practical applications.

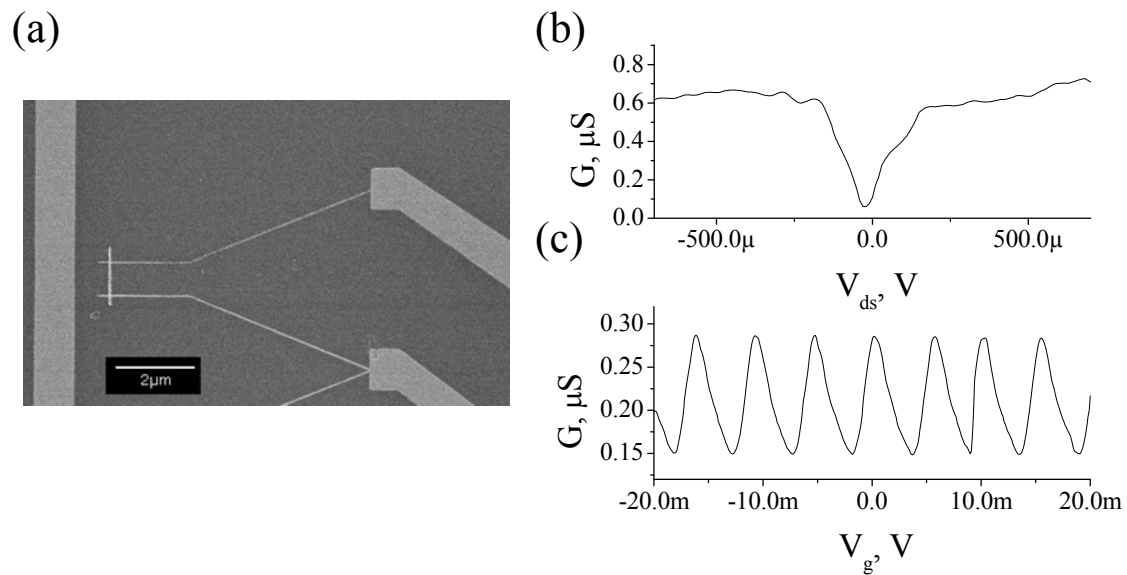


Figure 1 (a) SEM micrograph of the SET after fabrication (b) I - V_{ds} and (c) I - V_g characteristics taken at 0.33 K.

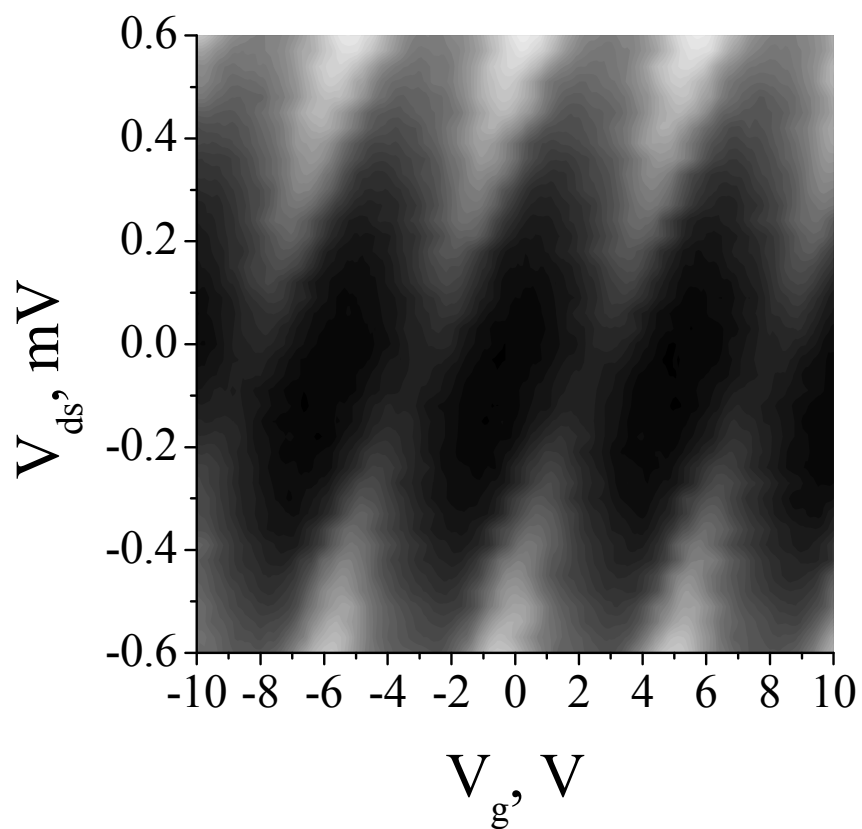


Figure 2 Charging diagram of the Pt SET with ALD dielectric.