Hybrid Lithography (E-beam/DUV) and Dedicated Etching Process for CMOS-compatible Monoelectronic Studies with Gates down to 12 nm

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Within the last decades, transistor dimensions were shrunk to a few nanometres. For those dimensions by modulating the access resistance of the device, it has been demonstrated channel can acts as a silicon quantum dot coupled to the gate and resistive access as a tunnel barrier [1]. For the purpose of the European project AFSID (Atomic Functionalities in Silicon Devices) [2] it is required to build a platform enabling the study of both single dopant transport [3] and coupled dots in multi gate devices [4] (fig 3). Respectively ultra short dimension and aggressive pitch are needed for these two different studies. Taking advantage of the capabilities of the LETI clean-room, a SOI CMOS-compatible platform [5] has been designed for that purpose, with optimised lithographic and etching processes.

We aim to combine ultra short and narrow device with multi-gate device on the same wafer. This platform was highly complex to obtain with regard to the device dimensions (see Fig. 1, device width at 31 nm) – and innovative device architectures requiring sub 100 nm pitch (see Fig 2, and Fig 3 with a pitch equals to 90 nm). Furthermore, a very accurate alignment control of the different lithography layers (overlays under 30nm) was necessary, particularly between the active area and the gate patterning (Fig. 3). For this purpose, we used hybrid lithography (e-beam/DUV), via the use of chemically amplified resists (CAR) [6, 7]. The e-beam exposures were carried out on a Gaussian electron beam writer (Leica VB6-UHR from Vistec) operating at 100KeV, allowing to produce a spot size of about 4 nm. In order to reach all the devices on the same wafer we added datatypes and proximity effect corrections were tested.

If the active level was etched at 20 nm through a thin SOI film, gate level is more challenging due to topography, requiring "over-etch" process. Nevertheless 12 nm poly-silicon gate has been etched with a 15 nm HTO (High Thermal Oxide) hard mask (fig 4). For that purpose, we use an Inductive Coupled Plasma (ICP) reactor from Applied Material has been used with $HBr/Cl_2/CF_4$ chemistry for the Main Etch (ME) and $HBr/He/O_2$ for the overetch. The hard mask has been etched within the same sequence with CF_4 chemistry.

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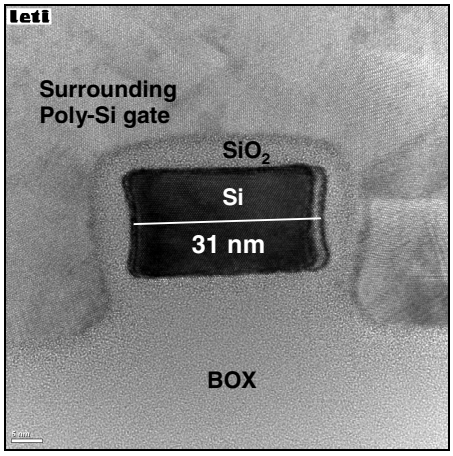

Fig 1: TEM analysis of a CMOS compatible SET (Single Electron Transistor) along the width. Active is 31 nm wide.

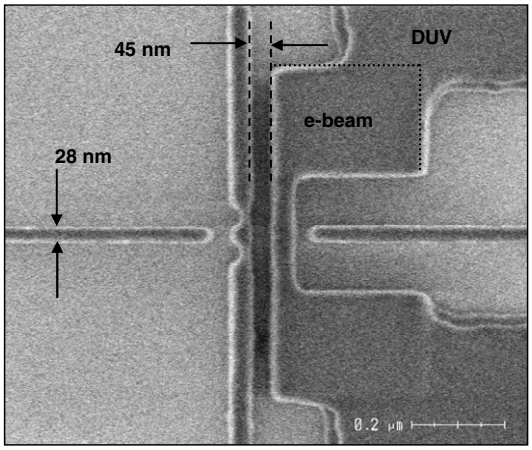

Fig 2 Single Electron Transistor (SET) with its detector. Space between lines is 45 nm.

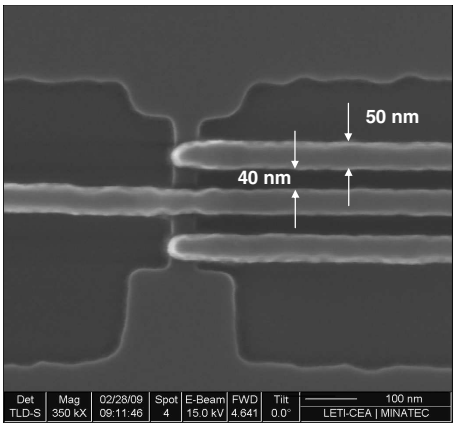

Fig 3 : Multi Gate device after gate etching process. Pitch is 90 nm.

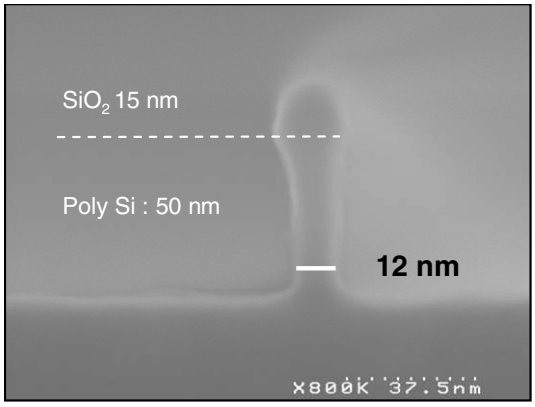

Fig 4: 12 nm poly-silicon gate.