Experimental Demonstration of Hybrid SET-CMOS Circuits

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As CMOS nears the end of scaling, the electronics industry is looking to alternatives to CMOS for high speed operation with low power computation. The use of Single Electron Transistors (SETs) in conjunction with advanced technologies such as Quantum-dot Cellular Automata (QCA) may provide an avenue for increased computational abilities beyond the CMOS paradigm. It is likely that future high performance computers will utilize QCA, SETs, or another new technology for high speed computing, due to the prohibitive energy demands of CMOS. However, the advantages of CMOS cannot be ignored. It is a well-understood, mature technology that is adequate in the majority of its current uses. CMOS will continue to be used in applications that require lower speed, including input and output systems for computers. Therefore, in order to harness the abilities of SET/QCA architectures, it is imperative to develop integration between SETs and CMOS architectures.

We have experimentally demonstrated the integration of a metal-oxide SET with a CMOS amplifier. The demonstration system consists of two major components: a single electron transistor, and a CMOS amplifier. The SET is fabricated of Al/AlO_x lithographically defined in MMA/PMMA using e-beam lithography. The SET has a separate gate that gives control of the electron population of the SET island. The source-drain voltage for the SET is applied through a large resistor. The changes in conductance of the SET as a result of gate modulation causes changes in the voltage drop across the SET. This voltage signal is fed to the input of the CMOS amplifier.

Two different CMOS voltage amplifiers were designed and fabricated for the SET readout: A CMOS linear amplifier with off-chip source and drain resistors, and a CMOS inverter, which provides gain with no external components. In both cases the amplifier was coupled to an SET situated on the same substrate. Since the SET must operate at temperatures less than 4.2K, the CMOS amplifier must also operate at this temperature. The amplifiers have been designed to operate at voltages of $<2V$ V_{dd}, to ensure that the transistors will not be significantly affected by the low temperature kink effect. The amplifiers must also have minimal power dissipation to ensure that the temperature of the sample can be maintained.

Testing of both the linear and CMOS amplifiers demonstrated amplification of the SET voltage output. Coulomb blockade of current in the I-V characteristic of SET and Coulomb blockade oscillations were observed with these amplifiers. For preliminary testing the SET-CMOS chip was tested on the cold finger of an He^3 Cryostat, and no significant temperature change of the He^3 pot was observed. The entire system functions at 400mK, demonstrating proof-of-concept of the use of CMOS and SETs together. We are currently optimizing our SET designs to achieve robust 4.2K operation.

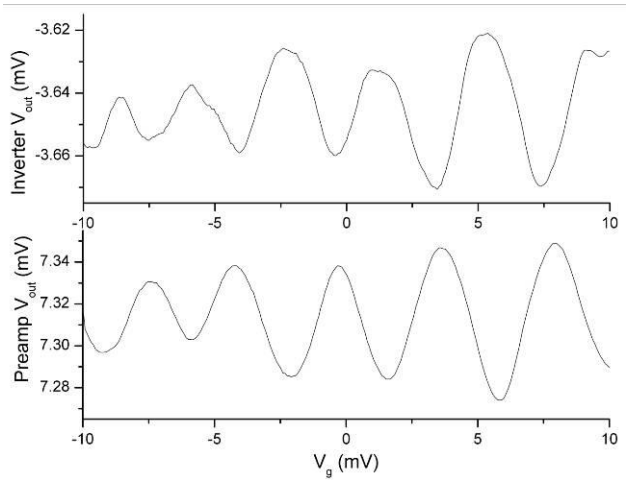

Figure 1: SET voltage divider output as amplified by (a) the CMOS inverter, and by (b) an external noninverting amplifier.

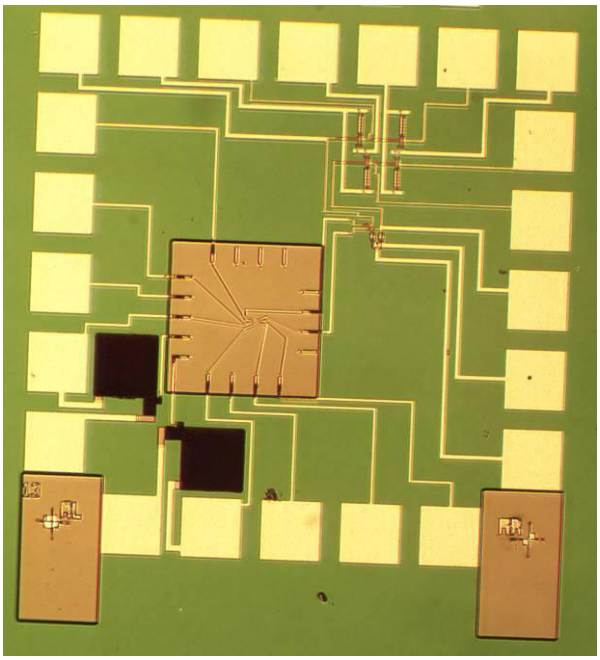

Figure 2: Complete SET-CMOS system. SETs are located in the center square, and the CMOS inverter can be seen in the top right.

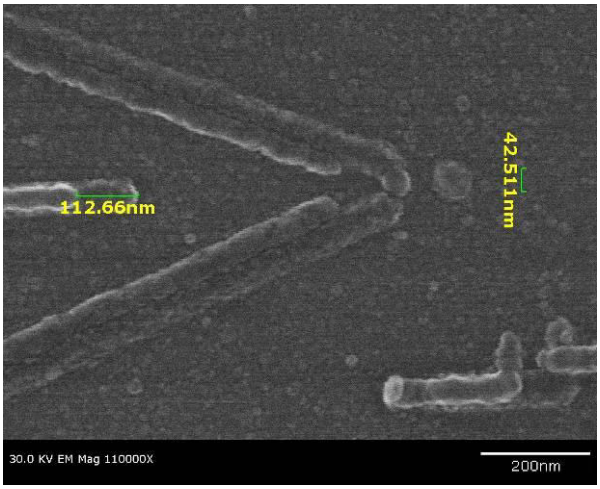

Figure 3: Aluminum-aluminum oxide single electron transistor fabricated on the silicon substrate, connected to the CMOS inverter