A low damage fully self-aligned gate-last process for fabricating sub-100 nm gate length enhancement mode GaAs MOSFETs

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High mobility channel materials based on III-V semiconductors are attracting significant attention as a route to enabling continued scaling of CMOS at, and beyond the 15 nm technology generation [1]. To be exploited, III-V MOSFETs must be realised using silicon manufacturing methodologies, which imposes significant constraints in terms of process induced damage. This work reports a self aligned dummy gate process flow which avoids subjecting the access regions of the III-V MOSFET to potential damage from etching of blanket deposited gate metal (which can be a significant issue for high work function gate metals such as Pt which can only be etched using strong physical biased processes) and in addition, gives significant freedom in gate metal choice for work function engineering. The complete flow, shown in Fig. 1, uses high resolution resist dummy gates defined, in this case on high-κ $Ga_xGd_yO_z$ (GGO) gate dielectric layers (though it should be stressed the process is generic to any high-κ III-V gate dielectric) followed by low damage dry etch modules and final gate metallization, with no critical dimension lift-off processes required. Initially, dummy gates are formed in NEB31 negative tone resist by electron beam lithography. Subsequently, a conformal layer of 300 nm SiN was deposited at room temperature, which formed the sidewall spacers after anisotropical low damage dry etching in an SF_6-based chemistry. Source and drain contacts were formed by first opening a large resist window centered around the gate, dry etching the exposed dielectric layer in a $SiCl_4$ chemistry [2], and subsequently blanket depositing an AuGeNi ohmic contact. To define individual source and drain contacts, the wafer was planarized with resist following a room temperature SiN layer deposition to prevent any possible short circuit between source/drain contact and gate metals. An using O_2 dry etch resist etch-back process revealed the SiN interlayer (Fig. 2), which was subsequently removed using an SF_6 reactive ion etch to expose the ohmic contact metal on top of the gate which was removed by further $Ar/O_2/SF_6$ reactive ion etching. Next, the resist dummy gate is removed by low damage O_2 dry etching process and the gate metal blanket evaporated

(Fig. 3). Subsequent planarization and etch-back using similar processes to those outlined above are employed to complete device fabrication.

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[1] http://www.itrs.net/Links/2007ITRS/Home2007.htm
[2] X. Li et al., Vac. Sci. Technol. B, 27, pp 3153-3157, 2009

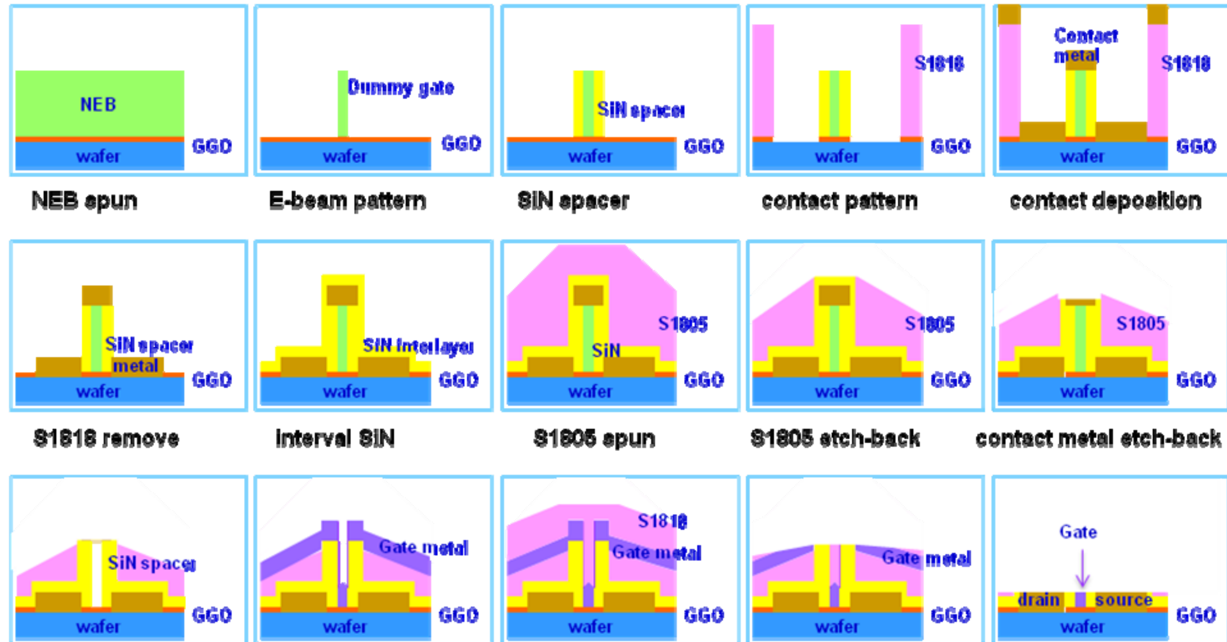

Fig. 1. Fully self-aligned gate-last process flow chart for fabricating sub-100 nm enhancement mode III-V MOSFETs.

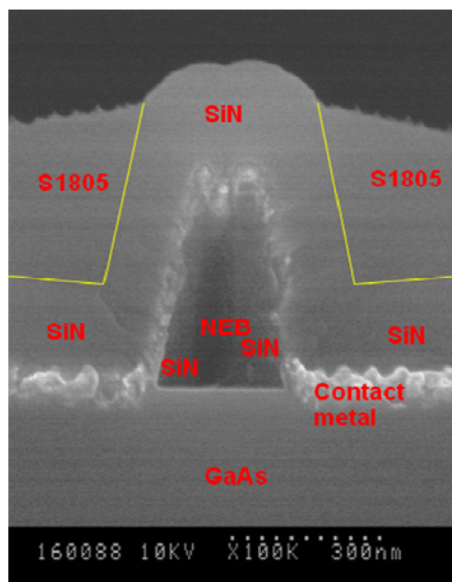

Fig. 2. SEM picture to show the opening of SiN and ohmic contact metal on gate top.

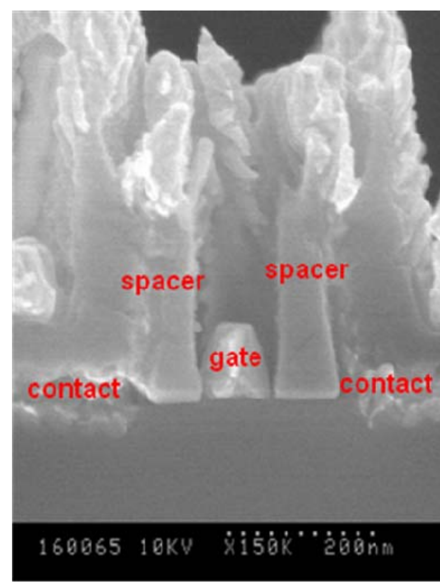

Fig. 3. SEM picture to show the gate metallization by replacing resist dummy gate.