Si Single Electron Transistor Fabricated by Chemical Mechanical Polishing

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Silicon Single Electron Transistors (Si-SET) have not only shown superior charge stability compared to metal junction devices, but the fabrication takes advantage of the maturity in silicon processing to scale down the dimensions to produce a smaller device that operates at elevated temperatures. However, most Si-SETs processes producing high charging energy devices, used by other researchers, have shown little control over the formation of islands and tunnel barriers [1]. The randomness in the process results in low yield and is therefore less likely to be implemented at a large scale.

Following our initial success in a newly proposed Si-SET fabrication method [2], we report the results of several process improvements. Starting with a degenerately doped silicon-on-insulator (SOI) wafer, very thin lines were defined by electron beam lithography using HSQ with enhanced contrast [3] and high resolution (~15nm). Silicon dioxide followed by nitride was uniformly deposited in by PECVD and polished by chemical mechanical polishing (CMP). The over-layer of LPCVD nitride was deposited on top of the oxide to improve uniformity and dishing in CMP as shown in Fig. 1(a) and (b). A perpendicular line on ZEP 520A was defined in EBL and etched in ICP with high silicon to oxide selectivity to separate the rib. In Fig 1(c) to (f), 1.5 nm of tunnel oxide was formed by rapid thermal oxidation and the remaining pit was filled with LPCVD amorphous silicon doped in phosphorous solid-state-diffusion. The SET's island was formed by a CMP step, with a high silicon to oxide selectivity, to remove the silicon over-burden, and the island was further thinned down by over-polishing.

Fig 3 shows the SET's charging diagram, demonstrating a charging energy of around 20 meV. From the shape of the diamonds, the source/drain junction and gate capacitances can be extracted as approximately 2 aF and 0.112 aF, corresponding to an island size of 13nm(HSQ) x 35nm(ZEP) x 8nm (SOI final thickness). The two gates, with gate-to-island distance of 200 nm in the layout, give 0.088 aF capacitance. The anomalies such as missing and split diamonds in charging plot and significant random telegraph signals (RTS) suggest that nearby traps, such as donor sites, play an important role in the transport characteristics so the device acts as a "Colomb glass".. Several fabricated SETs show Coulomb blockage (CB) oscillations at 4 K similar to Fig 4, demonstrating a reasonable yield for the process.

REFERENCES

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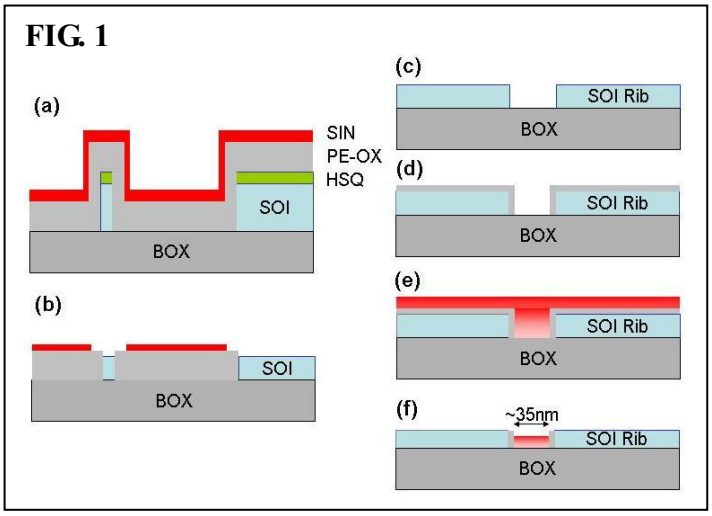

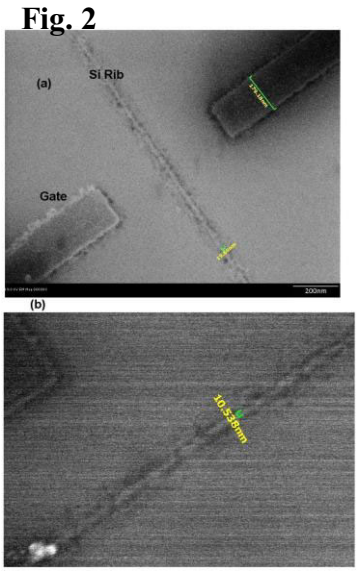

Fig. 1 Overview of the fabrication. In (a) and (b), the over-layer nitride on top of the PECVD oxide improves CMP planarization. The pit's sidewall was oxidized (d), filled with doped a-Si (e), and polished in CMP (f) to form a small island.

Fig. 2 SEM images of the polished sample after the final CMP. Very thin SOI rib (~15nm) and gates are embedded in PECVD oxide

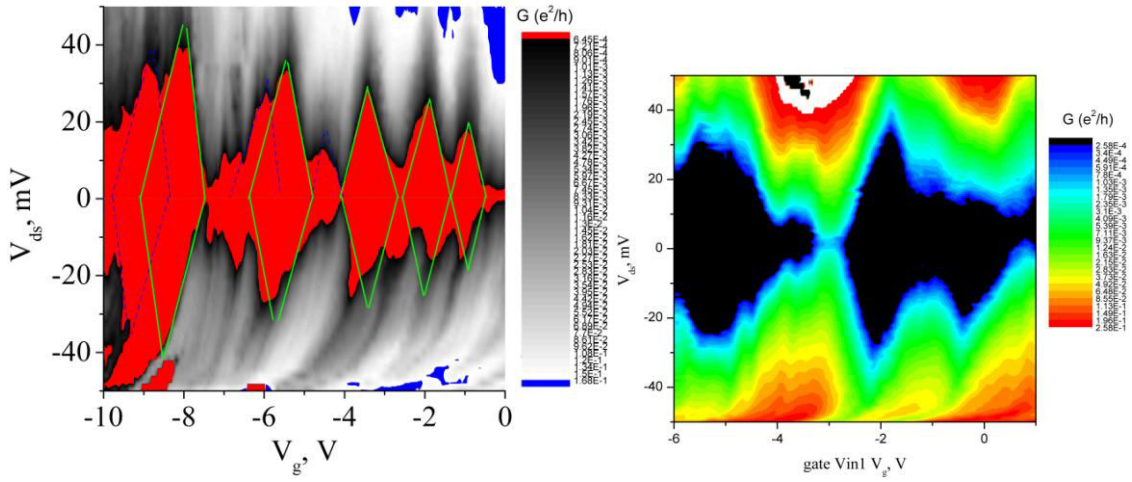

Fig. 3 Charging diagram of the fabricated Si-SET measured at 4K

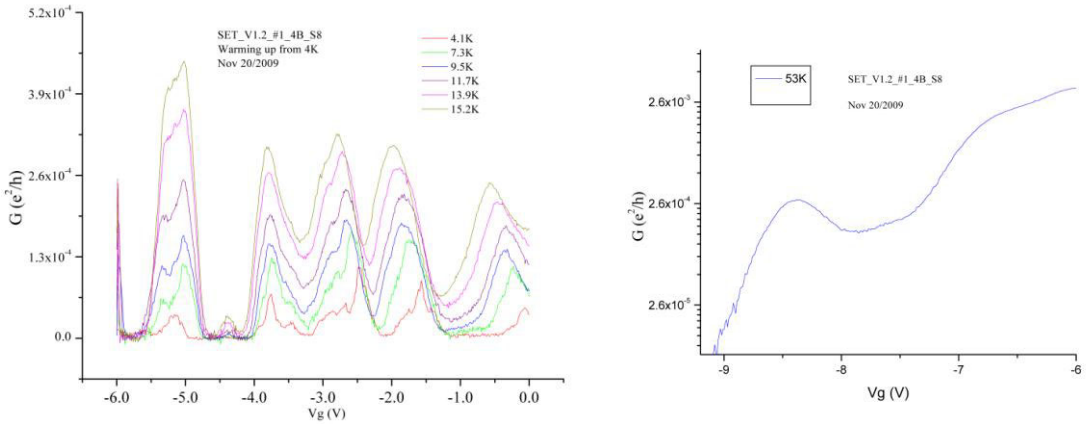

Fig. 4 Coulomb Blockade Oscillation (CBO) measured at various temperature from 4K to 15K (left), and at 53K (right)