Diblock copolymers technology for silicon nanowires/nanodots elaboration

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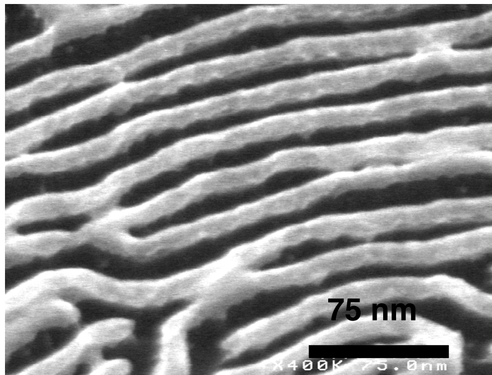
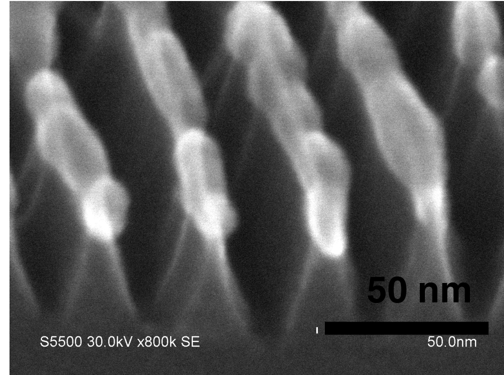
Nanomaterials are promising candidates for some of the basic building blocks in microelectronics, photonics, chemical sensors, solar cells and biology. The control of their shape, size, position and organization still needs to be solved for reproducible integration in functional devices. In this context, our strategy is a bottom-up one based on self-assembling properties of diblock copolymers systems to build regular patterns of nanodots and nanowires with dimensions from 5 to 50 nm. The original pattern of nanocylinders is made by spin-coating of PS-b-PMMA solution on Si substrate followed by an annealing step. Deep-UV and chemical treatments remove the PMMA cylinders and form a PS mask.[1]
A remaining challenge to use this technology in CMOS process is the difficulty to transfer the copolymer patterns in Si due to the very thin layer of PS mask (about 15 nm).[2] In this work, we present two original strategies to form a hard mask from PS pattern. This hard mask is then transferred into 40-100 nm thick Si layer by plasma etching. The first method is based on the high etching selectivity between a-SiO2 and a-C (amorphous C) with CF4 or HBr/Ar/O2 plasma to form an a-C hard mask. To reproduce the initial pattern in 60 nm thick Si layer (fig. 1.a), we have developed a dedicated plasma etching process. In the second strategy, we deposit directly a very thin (5 nm) specific hard mask material covering the PS matrix and remove the PS with an Ar/O2 plasma. After optimizing the plasma etching steps, 40 nm thick horizontal Si nanowires or 60 nm thick Si nanodots are formed (fig. 1.b,c). In comparison with the first method, this one produces the reverse pattern.
To take advantage of these very promising techniques, we have developed graphoepitaxy to align cylinders by mechanical confinement (fig. 1.d). Therefore, associating graphoepitaxy and etching strategies, we will show the possibility to fabricate silicon nanowires field effect transistors on SOI wafers and present some electrical characterisation. This method is (i) a large scale one, (ii) compatible with CMOS process and (iii) applicable to other type of materials (III-V and II-VI semiconductors, magnetic materials…).

[1] K. Aissou, T. Baron, M. Kogelschatz, A. Pascale, Macromolecules 40, 5054 (2007)
[2] C. T. Black et al. Applied Physics Letters 79, 409 (2001)



(a)



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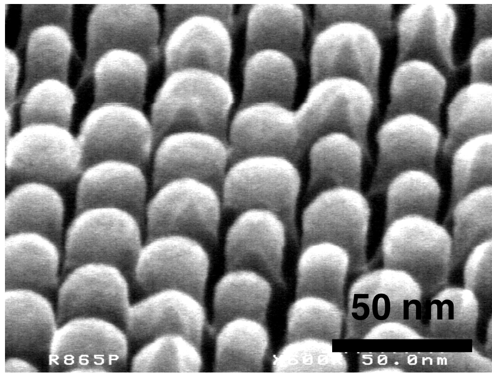
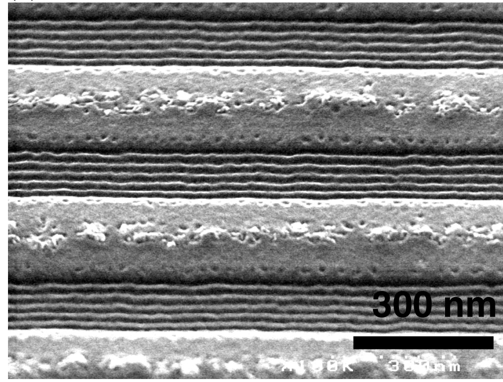


(c)



(d)

Fig 1. Silicon nanowires transferred (a) by etching of multi-layer substrate, (b,c) by using a lift-off process. (d) Alignment of PMMA cylinders by graphoepitaxy technique.