Nanometer scale Bosch process silicon etching

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Nanometer scale patterning by electron beam lithography (EBL) usually requires the use of thin resist to minimize the effects of forward scattering and also resist collapse with increasing aspect ratios. A typical subsequent process to EBL patterning is ICP etching of silicon. Many silicon etch processes which have good pattern transfer have limited selectivity with polymer resists such as PMMA and ZEP520. Therefore the depth which can be etched in silicon can be limited to less than the resist thickness.

The widely used Bosch process[1] has great selectivity but too much undercutting and scalloped sidewalls for nanometer scaled features. Alternatively, hard masks can be used with non Bosch etch processes, whereby the pattern in resist is transferred to another material, such as silicon dioxide, which has better etch selectivity to silicon. This solution is usually successful and is often used. However, it is extra processing and it would be more efficient if the silicon could be etched directly. Recent papers have extended Bosch etching to smaller features by shortening etch and passivation cycle times, lower gas flow, and lower RIE power[2,3]. Other approaches include incorporating oxygen in some manner to produce a thin oxide layer in order to minimize undercutting[4,5]. However, the smallest dense features reported so far are 100 nm trench and 70 nm space[6].

This work is unique in that the Bosch process has been modified to successfully etch a 60 nm pitch grating structure, which is almost a factor of 3 smaller than previous work. A 30 nm line and space CAD pattern resulted in a 33 nm exposed space and 27 nm resist line in 60 nm thick ZEP520 resist (Fig. 1). EBL exposure conditions were 240 uC/cm^2, 100 kV, 2 nA, and 5 nm shot pitch using a JEOL JBX-9300FS. Develop conditions were 30 sec immersion in amyl acetate at 21 C with isopropanol rinse. The pattern was then etched with an STS Multiplex ASE ICP etch system with 20 W RIE power at 380 kHz, 600 W coil power at 13.56 MHz, 5 sec etch cycle with 20 sccm SF_6, 6 sec passivation cycle with 50 sccm C_4F_8, and 6 mTorr chamber pressure. These process conditions achieved an actual 43 nm trench and 17 nm fin in silicon (Fig. 2,3), thus a 5 nm per side undercutting from the resist pattern. The aspect ratio of the silicon fins are 24 to 1 with a 3σ edge roughness of 3.9 nm. The etch rate is 27 nm / cycle and the selectivity of silicon to resist is 11 to 1.

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[1] F. Laermer and A. Schilp, U.S. Patent No. 5,501,893 (26 March 1996).
[2] Q. Li, L. Zhang, M. Chen, S. Fan, A process study of electron beam nano-lithography and deep etching with an ICP system, Sci China Ser E-Tech Sci, Jun. 2009, vol. 52, no. 6, 1665-1671.
[3] X. Wang, et al., High aspect ratio Bosch etching of sub-0.25 um trenches for hyperintegration applications, J. Vac. Sci. Technol. B 25(4) Jul/Aug 2007, 1376.
[4] J. Ohara, Y. Takeuchi and K. Sato, Improvement of high aspect ratio Si etching by optimized oxygen plasma irradiation inserted DRIE, J. Micromech. Microeng. 19 (2009) 095022.
[5] F. Ayazi and R. Abdolvand, An advanced reactive ion etching process for very high aspect-ratio sub-micron wide trenches in silicon, Sensors and Actuators A, 144 (2008) 109–116.
[6] C. Chang, et al., Etching submicrometer trenches by using the Bosch process and its application to the fabrication of antireflection structures, J. Micromech. Microeng. 15 (2005) 580–585

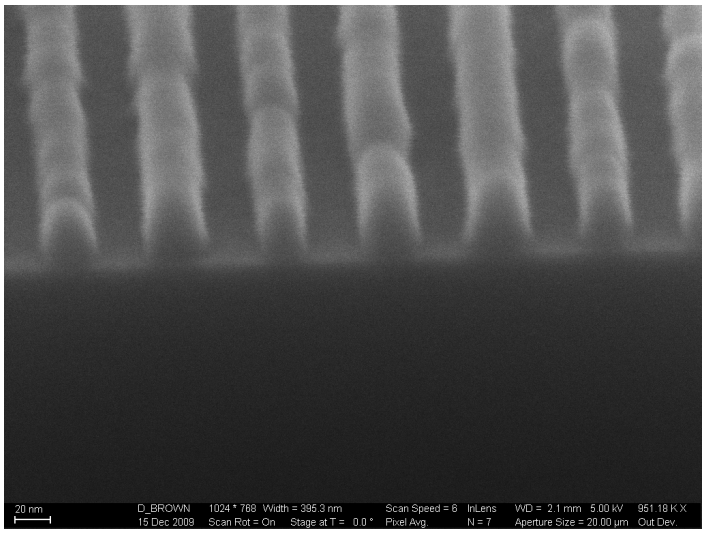

Figure 1: 60 nm pitch grating in ZEP520 resist prior to etching

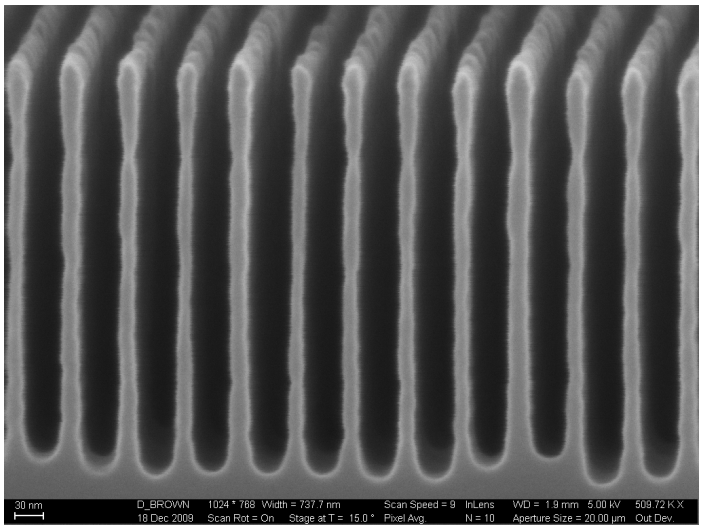

Figure 2: 60 nm pitch grating etched in silicon at 509 k magnification

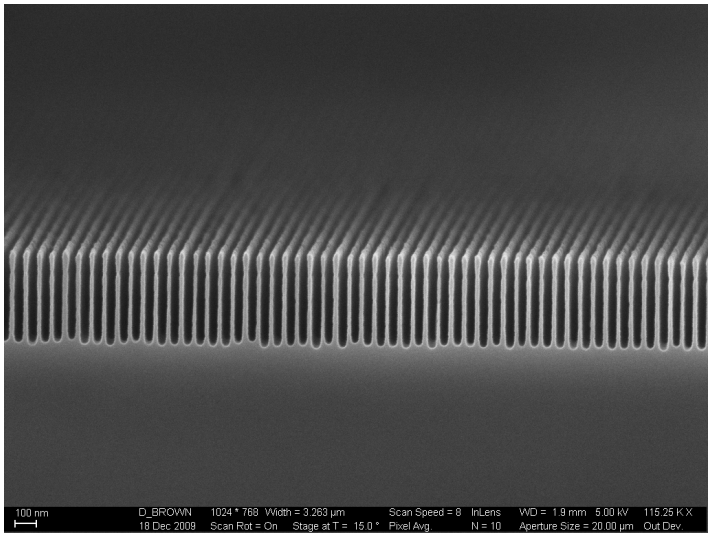

Figure 3: 60 nm pitch grating etched in silicon at 115 k magnification