Copper–plated 50 nm T–gate fabrication

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The emergence of projects such as COSMOS [1] is driving the monolithic integration of compound semiconductors and silicon materials to enable the exploitation of "more than Moore" solutions where bandwidth and power consumption are vital performance metrics. Key to full exploitation of heterogeneous materials integration of this type will be the ability to process III–V materials and devices in a standard silicon CMOS environment. This requires the development of gold–free metallisations and fully subtractive device process flows.

The outstanding high frequency and low noise performance of III–V HEMTs is currently enabled by the use of gold–based T–gate structures. Typically this structure is achieved using electron beam lithography, metal evaporation and lift–off, however this limits the minimum foot geometry to around 20 nm due to the thicknesses of resist required and the resulting beam spreading [2]. For silicon processing compatibility of T–gates, gold needs to be swapped out, and replaced with an alternate low resistivity material – an attractive solution is copper.

In this paper, we report for the first time, a route to the realisation of a scalable, sub–100 nm Cu–based T–gates using a fully subtractive, silicon compatible process flow.

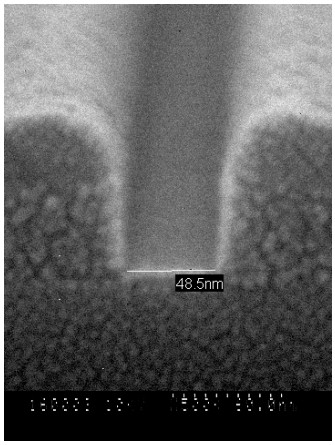
Initially, a 50 nm layer of ICP–CVD silicon nitride (SiN) is deposited on the wafer at room temperature. Next a 50 nm line is transferred into the SiN using a damage free SF_6–based etch [3] and ZEP 520A resist, patterned with a Vistec VB6 UHR EWF e–beam tool operated at 100 kV (Figure 1a). Following dry etch, the ZEP 520A resist is removed in Microposit 1165 solvent. A gate recess etch is then performed on the underlying semiconductor material using the trench etched in the SiN as a mask (Figure 1b). Next a 30 nm/30 nm Ti–Pt film is blanket evaporated. This fills the 50 nm trench in the SiN and in addition covers the rest of the wafer, and as such, this metal film acts as the Schottky gate contact to the underlying semiconductor, the seed layer for the copper plating, and as a diffusion barrier to the copper [4]. Next, the wafer is coated with PMMA, and a gate head, patterned by e-beam lithography, aligned to the gate foot. Development of the PMMA reveals the underlying Ti–Pt plating base. The copper gate head is plated using a solution of $CuSO_4$, H_2SO_4, NaCl, $C_3H_7NaO_3S_2$ (an accelerator), polyethylene glycol (a suppressor) and CH_4N_2S (a brightener), using a DC current of 100 mA for 90 s. This process has been optimised to enable the formation of 200 nm critical geometry features. The plated copper has a bulk resistivity of better than 40 $\mu\Omega$ cm. The PMMA is then removed and the unwanted Ti–Pt removed using a low–damage SF_6/C_4F_8 ICP etching process. A plated T–gate structure is shown in Figure 1c and the complete process flow is shown in Figure 1d.

[1] DARPA, "COmpound Semiconductor Materials On Silicon." http://www.darpa.mil/mto/programs/cosmos/index.html. accessed: January 2010.

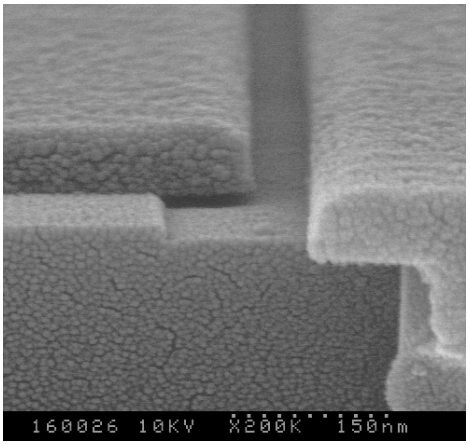
[2] S. Bentley, X. Li, D. A. J. Moran, and I. G. Thayne, "Two methods of realising 10 nm T–gate lithography," *Microelectronic Engineering*, vol. 86, no. 4–6, pp. 1067–1070, 2009.

[3] X. Li, R. J. W. Hill, H. Zhou, C. D. W. Wilkinson, and I. G. Thayne, "A low damage Si_3N_4 sidewall spacer process for self–aligned sub–100 nm III–V MOSFETs," *Microelectronic Engineering*, vol. 85, no. 5–6, pp. 996–999, 2008.

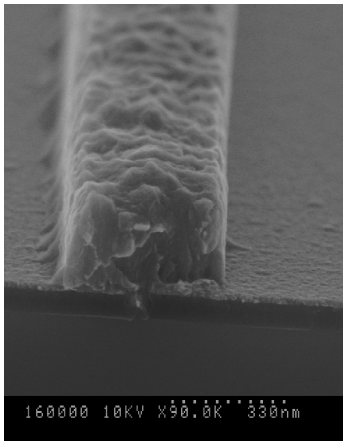
[4] S.-W. Chang, E. Y. Chang, C.-S. Lee, K.-S. Chen, C.-W. Tseng, Y.-Y. Tu, and C.-T. Lee, "A gold–free fully copper–metallized InP heterojunction bipolar transistor using non–alloyed ohmic contact and platinum diffusion barrier," *Japanese Journal of Applied Physics, Part 2: Letters*, vol. 44, no. 28–32, pp. 899–900, 2005.



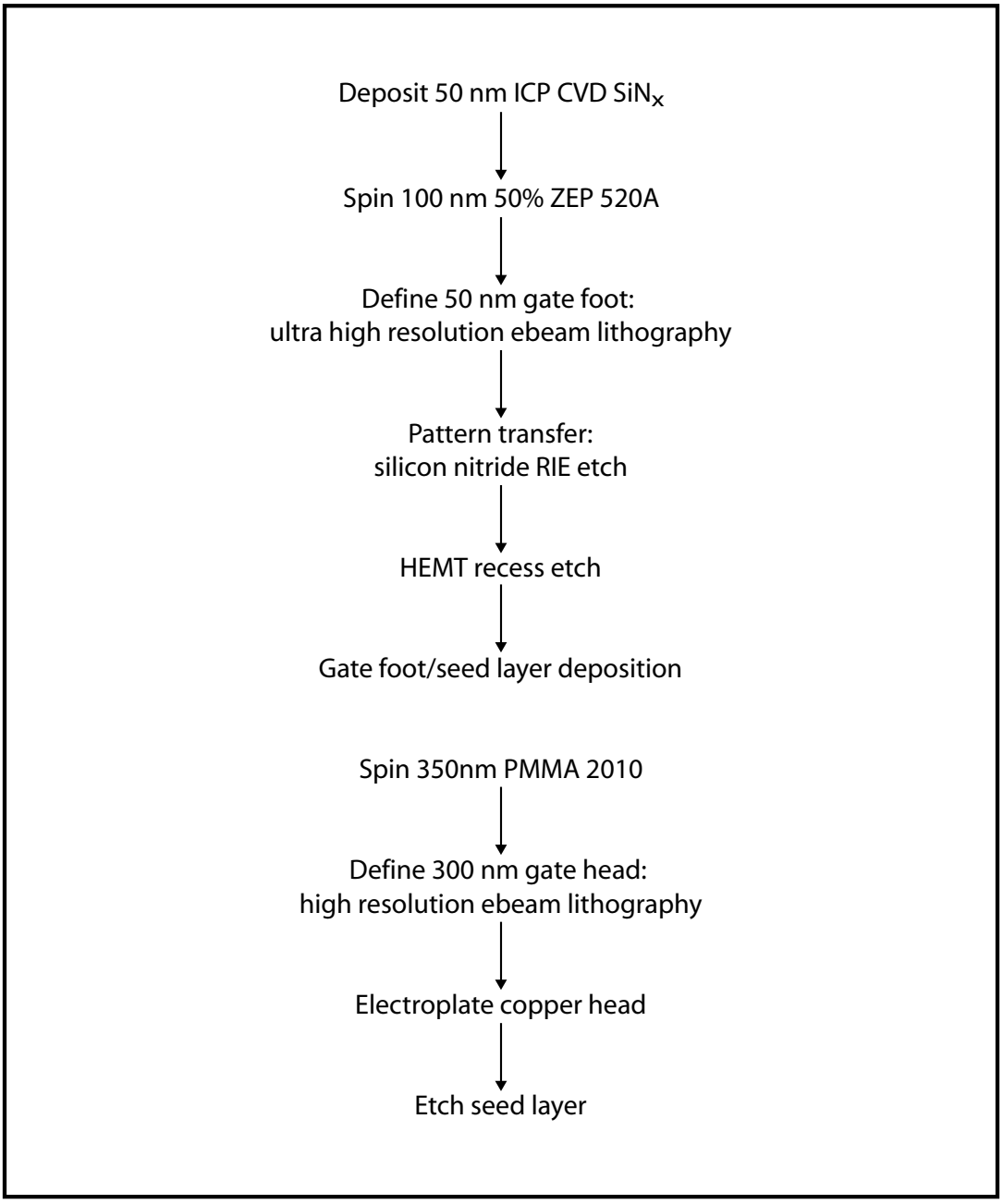
(a)



(b)



(c)



(d)

Figure 1: SEM of a 50 nm scale silicon nitride T–gate foot definition and support structure (a); SEM of recess etch masked by silicon nitride gate foot (b); SEM of 50 nm copper–plated T–gate structure (c); and the process flow for a 50 nm copper–plated T–gate structure (d).