Batch wafer fabrication of passivated carbon nanotube transistors for electrochemical sensing applications

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Since the operation of carbon nanotube transistors (CNT-FETs) was demonstrated [1], much progress has been achieved on the knowledge about electronic transport on SWCNTs and on their application for sensing [2]. However, a standard high yield technology to fabricate single SWCNT-FETs is still under development.

In this contribution we present a technological process for batch fabrication of SWCNT-FET based chips for electrochemical sensing applications. This technological process is based on a previously presented technology [3]. Fabrication of the SWCNT-FET structures is performed by using standard microelectronic steps at wafer level. Optical lithography is the only patterning technique to be used. The overall process can be divided in three main steps: substrate preparation, selective synthesis of the SWCNTs and definition of the metallic contacts, lines and pads. Recently, we have reported batch fabrication of 10,000 SWCNT-FET devices on a 4 inch wafer [4].

Application of SWCNT-FET for electrochemical sensing requires the devices to be passivated so that the CNTs, but not the metal contacts nor the lines, are exposed to the solution. With that purpose we have developed a post-fabrication passivation procedure of the SWCNT-FET structures. The procedure consists in a PMMA coating of the surface and an electron beam lithography (EBL) to locally remove the PMMA between the two metal contacts of the devices. EBL process is programmed to automatically align the pattern on each device. Additionally, it is performed at low electron beam energy to avoid any damage on the devices [5].

Figure 1a shows a batch fabricated wafer. The wafer contains 234 chips as the one that has been magnified in b. Each chip is formed by 6 SWCNT-FET structures, 1 back gate and 3 electrodes for electrochemical sensing. The wafer contain in total 5,616 CNT-FET sensing structures. Almost 30% of the devices on the wafer were identified as operative. One third of those devices showed a semiconducting characteristic. Figure 2 are SEM images of a passivated SWCNT-FET device. The lower in magnification SEM image shows the device, the automatic alignment marks and the EBL pattern. The higher in magnification image shows the patterned 1μm wide trench in between the 1.5 μm gap of the device. In this case the device is composed of two SWCNTS. Figure 3 shows the electrical characteristics of a device before and after the passivation/depassivation process. The performance of the device is preserved.

Passivated SWCNT-FET devices are currently being tested in electrochemical environment.

[1] R. Martel et al., Apl. Phys. Lett. 73 (1998) 2447; S.J.Tans et al., Nature, 393 (1998) 49.
[2] M. S. Dresselhaus et al., Carbon Nanotubes: Synthesis, Structure, Properties, and Applications (2009), Springer.
[3] Y.C. Tseng et al., Nano Lett. 4 (2004) 123.
[4] I. Martin-Fernandez et al., Microelectron. Eng. (2009), doi:10.1016/j.mee.2009.11.026.
[5] G. Rius et al., Microelectron. Eng. 84 (2007) 1596.

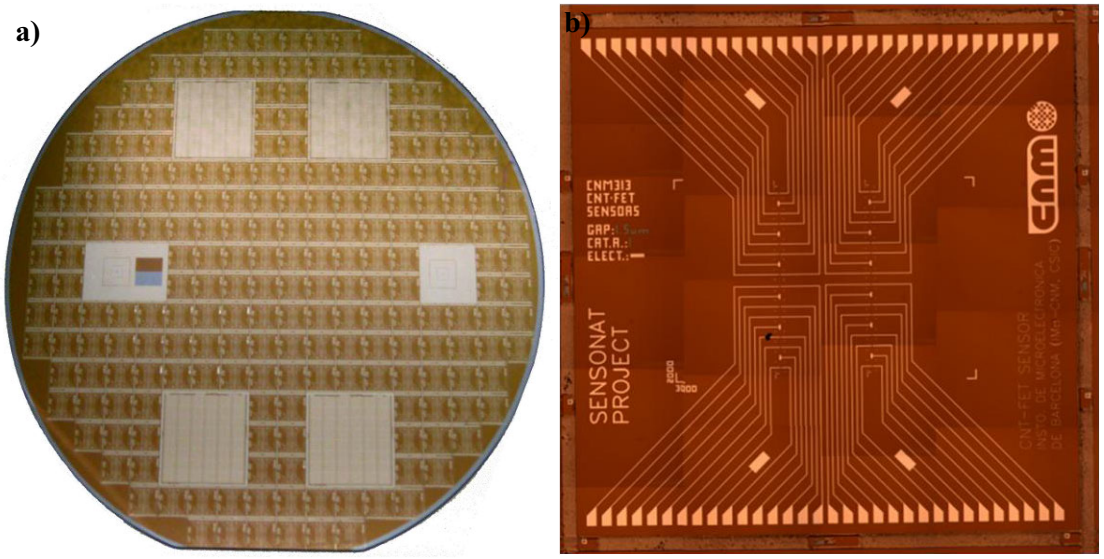

Figure 1: (a) Optical images of a batch fabricated 4 inch wafer containing 234 CNT-FET chips. (b) Optical image of one of the CNT-FET chips on the wafer. The chip is 5 mm x 5 mm.

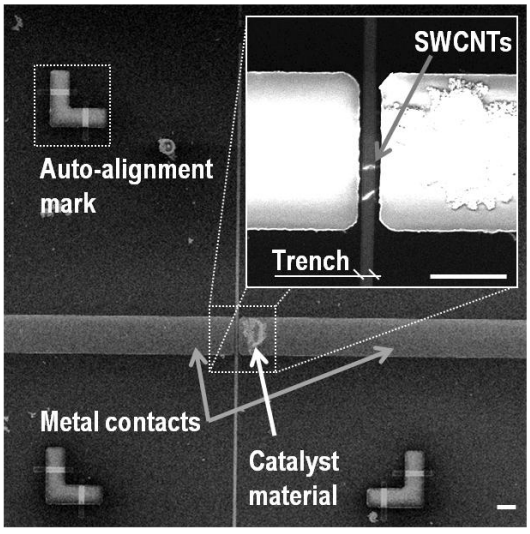

Figure 2: SEM images of a CNT-FET device area after the passivation/depassivation procedure. The inset shows the patterned between the metal contacts trench. Scale bars are 5 µm.

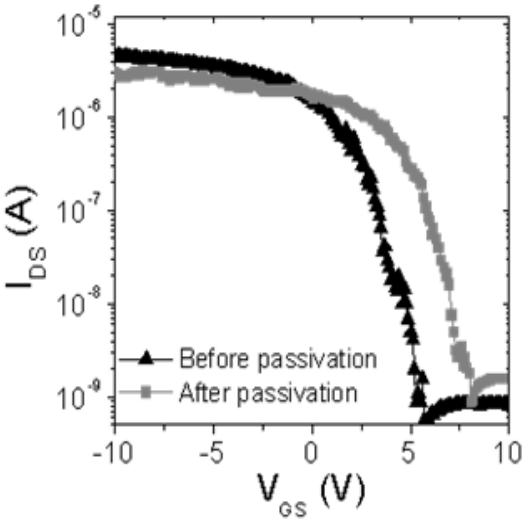

Figure 3: Drain-source current vs. gate voltage of a device showing a semiconducting characteristic before and after the passivation procedure. Drain-source voltage is 0.5 V.