Sub-30-nm patterning of Au on GaAs Substrates

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In this work, we demonstrate the patterning of Au features on <111> B GaAs substrates by galvanic displacement and metal evaporation into sub-30-nm pores in a silicon oxide hard mask layer. Patterning of small Au features onto GaAs substrates is of particular interest due to their use as metal catalysts for GaAs and GaAs-alloy nanowire growth. Semiconducting nanowires have a variety of potential applications, such as field-effect transistors (FETs) [1], and their size-dependent properties have been exploited for a variety of optoelectronic devices [2]. However, much work remains in creating lithographically-templated nanowires for integration into future manufacturing processes.

Au in particular has shown particular promise in producing oriented, size-selected nanowires [3]. While previous research by Berggren and Gradecak groups have significantly improved on the smallest lithographically-fabricated catalyst-particle size [4], unwanted nanowire growth prevented selective growth of nanowires, due to the migration of metal particles during the nanowire growth process, and the self-catalysis of GaAs nanowires from the GaAs substrate.

Samples were prepared using <111> B GaAs substrates with 30 nm of evaporated silicon oxide deposited on top. The samples were patterned by electron-beam lithography, using a PMMA resist, and developed via a cold

development process [5]. Pores were opened in the hard mask by HCF_3/CF_4 reactive-ion etching. After removal of the GaAs native oxide, metal catalyst nanoparticles were deposited into the pores by either electron-beam evaporation of Au, with a nominal thickness of 3 nm, or by galvanic displacement (GD) in a calibrated solution that also deposits 3 nm of Au. The GD solutions were prepared by dissolving hydrogen tetrachloroaurate(III) trihydrate (Alfa Aesar Co.) into deionized (DI) water. With either method, the sub-30-nm gold nanoparticles were fabricated.

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