Smooth Suspended Silicon Nanowires for Light Emission Applications

*Chookiat Tansarawiput, Lin Zhao, Leo T. Varghese, and Minghao Qi**

School of Electrical and Computer Engineering, and Birck Nanotechnology Center
Purdue University, West Lafayette, IN 47906

Silicon does not emit light easily due to its indirect band gap. However, when one or more of its dimensions shrink down to a few nanometers, the band diagram changes and a direct band gap emerges due to quantum confinement [1]. Visible light emission from chemically synthesized nanowires or quantum dots has been demonstrated [2]. However, such nanowires and quantum dots do not lend themselves to easy device integration.

While lithographically defined wires can go down to sub 10 nanometers, the line edge roughness may disturb the band diagram and promote other non-radiative recombination, thus reducing the light emission efficiency.

Here we propose to use orientation dependent etch on a silicon-on-insulator (SOI) platform to achieve suspended nanowires with smooth and uniform sidewalls. The diameters of the nanowires can then be reduced with thermal oxidation, and the oxide can also passivate the nanowires.

Our process starts with the thermal oxidation of an SOI wafer with an 80nm thick device Si layer of [110] crystal orientation. After HF dip, the remaining thickness of Si was 20 nm. Since the substrate is [100] Si, the crystal orientation of the top [110] layer cannot be identified observing the notch. An exposure of lines with a variety of directions followed by KOH etch was first conducted to find the crystal orientation of the top [110] Si layer. Then gratings of 100 nm, 60 nm and 40 nm pitches were written in HSQ with electron-beam lithography and the gratings were oriented with the [111] crystal orientation. Fig. 1a shows 20nm half-pitch grating exposed in 20nm thick HSQ. A high temperature annealing at 1000 °C in Nitrogen was performed to cure the exposed HSQ. The wafer was then immersed in KOH at room temperature and 5 minutes were sufficient to etch 20 nm of Si.

To suspend the Si nanowires, large pedestals of different separations were written to support the gratings (Fig. 1b and Fig. 2). The wafer was then etched in diluted HF for three minutes to remove the buried oxide. Fig. 2a and 2b show the top view and 30° tilted view of the 100nm pitch and 60nm pitch suspended gratings, respectively. The suspended gratings were straight and smooth. The current minimum line width is about 15nm. To further reduce the line width, thermal oxidation can be adopted. Figure 3 shows the process of thermal oxidation to reduce the line width by 10nm. The suspended nanowires allow one to thin down the nanowire uniformly around all four sidewalls. The smooth sidewalls should allow us to achieve narrow lines < 5nm without worrying that the lines might break due to line edge roughness.

We plan to implant and form *pn* junctions in the nanowires and measure the electro luminescence. In that case, the implantation will be done before the grating is suspended.

* corresponding author: Minghao Qi, 1205 W. State St, Rm 1297, West Lafayette, IN 47906
Email: *mqi@purdue.edu*

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[2] J. Huo, R. Solanski, J. L. Freeouf & J. R. Carruthers, "Electroluminescence from silicon nanowires", *Nanotechnology,* **15**, p1848-1850, (2004).

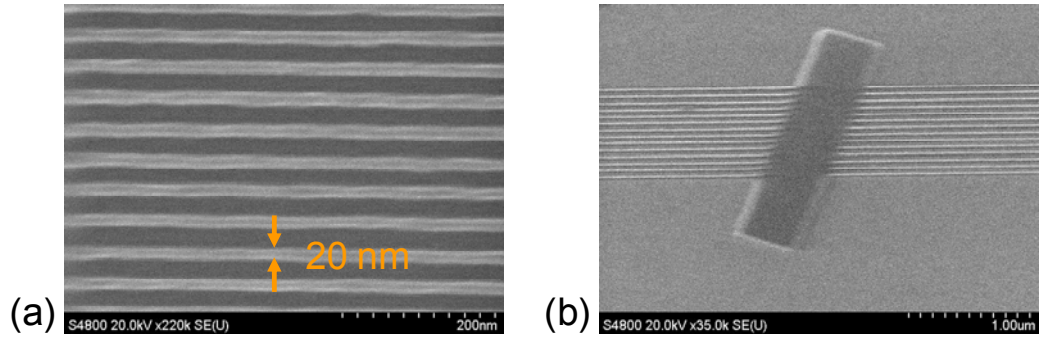

Fig. 1: (a) 20nm half-pitch grating exposed in 20nm thick HSQ. (b) Support structure for 60nm pitch grating after the KOH etch at room temperature

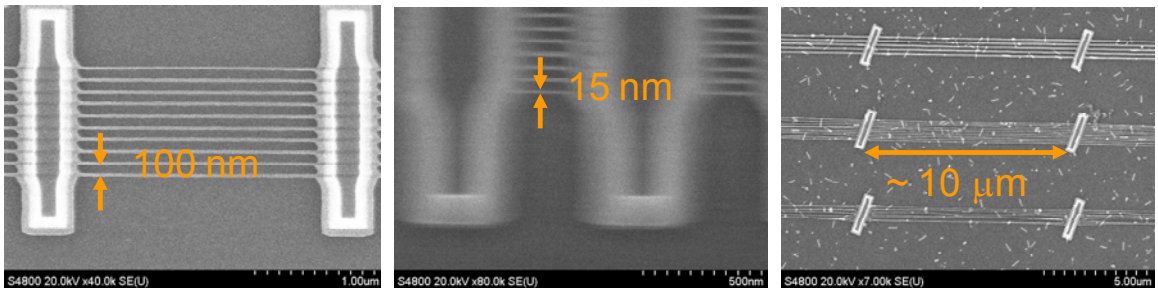

Fig. 2: Suspended nanowires after the HF dip. (a) 100nm pitch gratings. (b) Tilted top view of 60nm pitch grating. The width of wires is 15nm. To achieve longer suspended gratings, critical point drying (CPD) was applied. (c) Top view of 10 µm long free standing Si gratings. The grass is due to the contamination from the CPD machine

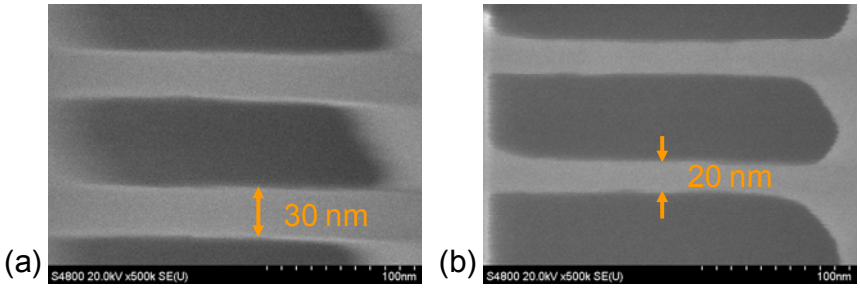

Fig. 3: The width of the nanowires can be reduced by thermal oxidation. (a) Before oxidation, the width is 30nm. (b) After oxidation for 95 min. at 800 °C, the width is reduced to 20nm. The thickness of the nanowire is also expected to decrease by 10nm.