Impacts of Point Spread Function Calibration Methods on Model-Based Proximity Effect Correction for Electron-Beam-Direct-Write Lithography

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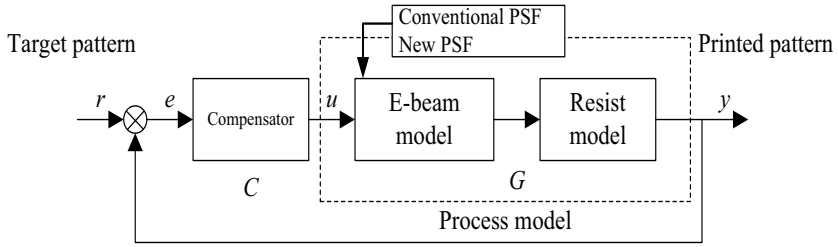
Electron-beam─direct-write (EBDW) lithography at lower electron accelerating voltages has been considered for the 22-nm half-pitch technology node and beyond. It requires lower resist dosage and induces less heating effects. Enhanced throughput, critical dimension control and overlay may be obtained comparing with higher voltages. However, the lower accelerating voltages cause significantly different energy deposition within resist, which may limit patterning fidelity. Previously, a new point spread function (PSF) calibration method has been developed to more accurately represent the proximity effects at 5-keV[1].

In this paper, a new model-based electron proximity correction (MBEPC) methodology based on model-based optical proximity correction[2,3] is presented. Impacts of PSF calibration accuracy on the MBEPC results are analyzed. An overall MBEPC block diagram is shown in Fig 1. It iteratively modulates layout geometry by feedback compensation until the correction error converges. Different energy intensity distributions are efficiently calculated by fast convolving the modulated layout with various PSFs. The effectiveness of the MBEPC methodology with various PSFs is quantified in terms of CD offset, corner-rounding, and line-end-shortening versus ITRS requirements[4]. Fig 2 shows an example of applying MBPEC to a conventional six-transistor-SRAM cell with a two-dimensional layout for the poly layer at 5-keV. The line CD target is 18 nm and the cell area size is 0.36 μm^2. Comparison of correction convergence for two PSFs calibrated by one conventional method and the new method respectively is shown in Fig 2(a). Improvements in reduced CD offset, corner rounding and line end shortening are shown in Fig 2(b), (c), and (d). After-correction patterning fidelity improvements of the new proposed and conventional PSF are 6.87 times and 3.02 times respectively in terms of normalized mean square error (NMSE) defined as a quantitative measure of overall pattering errors. The experimental verification is ongoing.

1 C.-H. Liu et al., in *Proceedings of SPIE* **7140**, p. 71401I (2008).
2 P.-L. Tien, MS Thesis, National Taiwan University (2007)
3 Y.-S. Su *et al.*, in *Proceedings of SPIE* **6924,** p. 69243Z (2008).
4 International Technology Roadmap for Semiconductors, "Lithography" (2009).



r: desired wafer pattern; *y*: printed wafer pattern; *e*: the difference between the *r* and *y*; *C*: feedback compensator; *G*: process model, including an E-beam model and a resist model

Fig 1: Overall MBPEC block diagram based on an OPC algorithm[2]

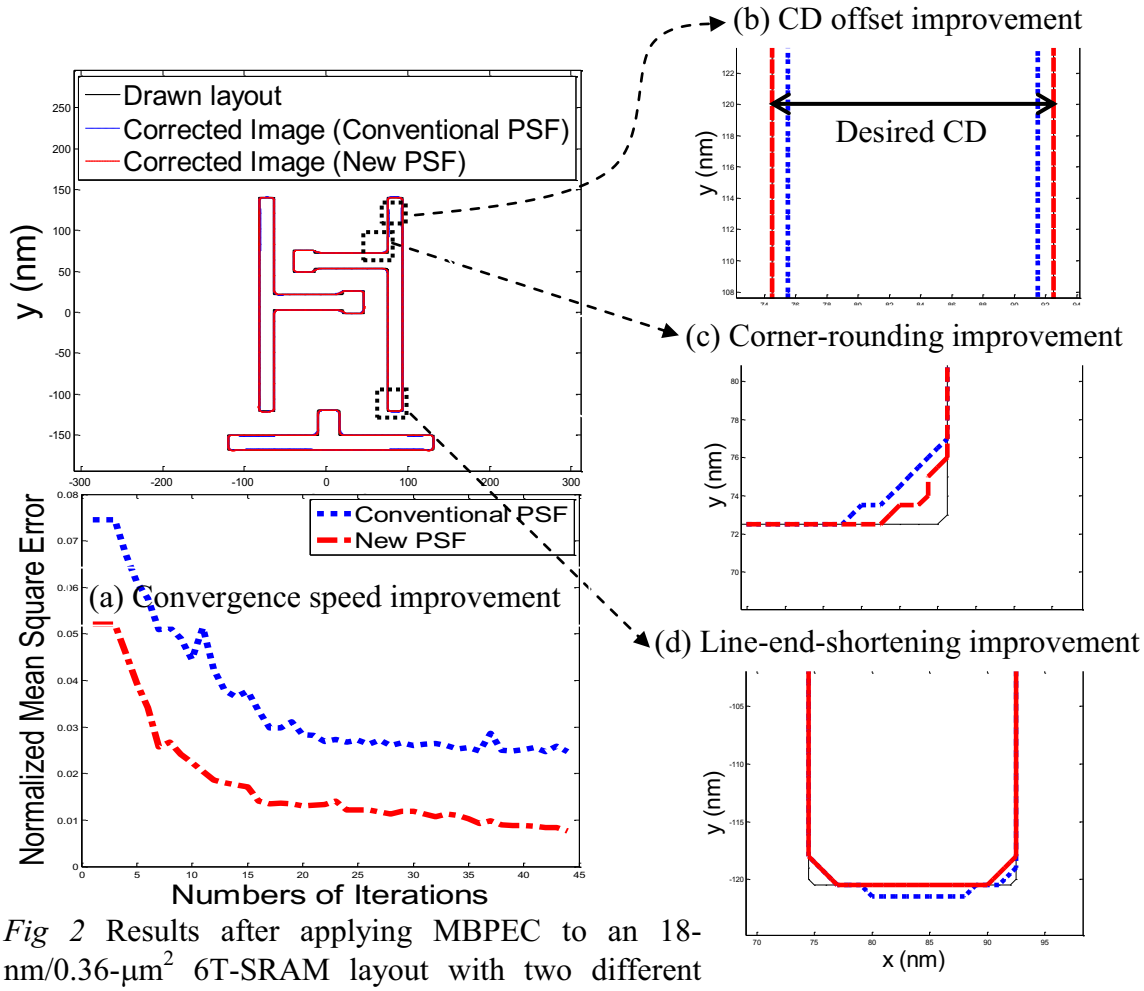


Fig 2 Results after applying MBPEC to an 18-nm/0.36-μm^2 6T-SRAM layout with two different PSFs.
Comparisons of (a) convergence speed, (b) CD offset, (c) corner-rounding, and (d) line-end-shortening