

Study of Transport Properties in Graphene Monolayer Flakes on SiO₂ Substrates

J. M. Tirado

EUITI Toledo, University of Castilla-La Mancha, Avda. Carlos III s/n, Fabrica de Armas, Toledo, Spain

D. Nezich, J. W. Chung, X. Zhao, J. Kong, T. Palacios

Department of EECS, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA, USA

Materials based on carbon nanostructures quickly becoming a feasible alternative to Silicon technology in future high speed electronic. Graphene, a single monolayer of sp²-bonded carbon atoms, turns out an ideal candidate for this application due to its excellent high mobility and Fermi velocity. In spite of these very promising properties [1], the development of graphene devices is still in a very preliminary stage and there are many unknowns about the reproducibility and transport properties of these devices [2]. Extrinsic scattering sources, many of which arise from the surface morphology, chemistry, structural, and electronic properties of the widely used SiO₂ substrate, limit the mobility of graphene devices by as much as several orders of magnitude with respect theoretical calculations [3]. Great effort is currently underway to increase the mobility beyond extrinsic limits.

In this work the transport properties of field effect transistors (FETs) fabricated on a graphene flake have been studied for a range of temperatures. In particular carrier mobilities in graphene for electrons and holes as a function of the vertical electric field are presented and compared to universal mobility curves in Silicon [4]. The dimensions of the graphene flake used in this work are 615 nm in length and 1450 nm in width. The graphene FET was fabricated on top of a Si wafer with a SiO₂ layer. The I-V characteristics were measured with an Agilent 4155A semiconductor parameter analyzer at different temperatures. In these measurements, the source-drain voltage is fixed to a constant value of 0.1 V. A back-gate step voltage is applied at the bottom of the sample, with a bias sweeping from -40 to 40 V and back again, in steps of 0.5 V.

Figure 1 shows the drain-current response while sweeping the gate voltage for the device at 300 K. The ambipolar nature of the graphene is clearly revealed in the figure. For gate voltages below 8 V, the conduction is due to holes while more positive voltages induce an electron current. Figure 2 shows the electron mobility extracted from Figure 1, compared to the universal mobility curve of Silicon. Although the excellent mobility of graphene is clearly seen at low vertical fields, at higher fields the mobility severely degrades and approaches the one in Si. Phonon scattering dominates but further work is needed to understand the origin of this important reduction.

References

- [1] A. K. Geim and K. S. Novoselov. The rise of graphene. *Nature Materials* Vol. 6, March 2007.
- [2] T. Pichler. Carbon ahead. *Nature Materials* Vol. 6, May 2007.
- [3] X. Hong, A. Posadas, K. Zou, C. H. Ahn, J. Zhu. High-Mobility Few-Layer Graphene Field Effect Transistors Fabricated on Epitaxial Ferroelectric Gate Oxides. *PRL*, Vol. 102, 136808, April 2009.
- [4] Z. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis. Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates. *IEEE Electron Device Letters*. Vol. 22, No. 7, July 2001.

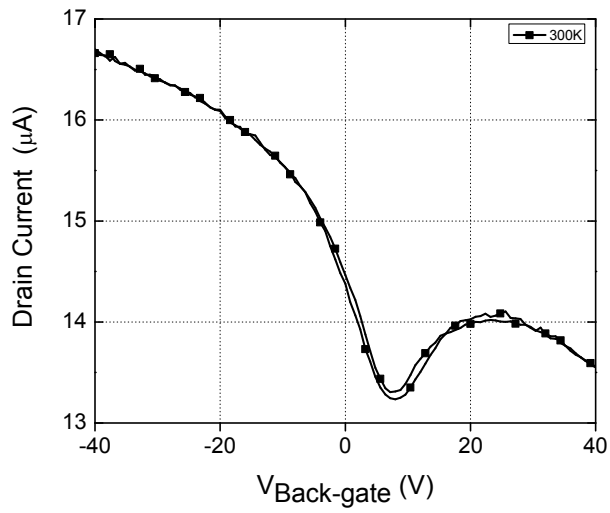


Figure 1: Drain current response of a back-gated graphene field effect transistor at 300 K. The back-gate voltage is swept from -40 to 40 V and back again in steps of 0.5 V. Drain-Source voltage was set to 0.1 V.

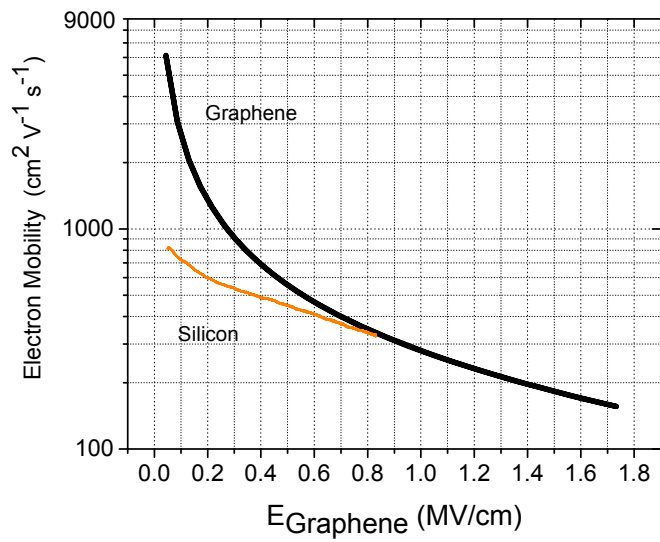


Figure 2: Universal mobility curve for Graphene compared to Silicon for a Temperature of 325 K