Mask Technology for Self-Powered Electron Lithography with sub-35nm resolution

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The reduction in critical dimension (CD), high-throughput and cost reduction of nano-lithography, are cruicial to developing commercially viable high performance nano-devices. Conventional optical lithography has high throughput due to parallel exposure mechanism, but the CD is limited by the optical wavelength. State-of-art electron beam lithography has the highest resolution, owing to small electron wavelength and low scattering cross-sections in e-beam specialized resists, but it suffers from the high cost and low throughput due to the required electron beam raster scanning serial exposure mechanism[1]. Our recently reported (published in EIPBN 2009) self-powered electron lithography (SPEL)[2], utilizing the spontaneously emitted energetic electrons from beta-emitting radioisotope thin-films, demonstrated 100nm gap between e-beam posts. SPEL enables vacuum less e-beam lithography, and circumvents issues with proximity effects and mask heating by simultaneous exposure, and exposure in air respectively.

Here, we further experimentally demonstrated a minimum 35-nm resist feature, by using a new mask fabrication technique in SPEL (Fig.2). A layer of *continuous* Si_3N_4 "opaque" supporting layer was used here for mask, instead of nitride that had been etched to form a stencil mask. The stencil mask prevents disjoint features, such as donut shapes, to be formed. In the new mask design, the continuous silicon-nitride and tungsten thin layer laminate is formed. Furthermore, the tungsten layer is etched partially to define the areas where electrons are transmitted to the photoresist.

The modulated tungsten thickness enables two major advantages. First the mask is mainly planar with little stress gradients, and a continuous electrically conductive layer allows for easy charge dissipation. The exposure modulation can be written as

$$J_{e\_out} = J_{e\_in} \cdot \exp(-\nu_1 \cdot \rho_1 \cdot h_1 - \nu_2 \cdot \rho_2 \cdot h_2) \quad (1)$$

Where J_{e_in} is the beta electron flux density from the source and J_{e_out} is the out flux density from the mask hole. ρ_1 and ρ_2 are the mass density of the supporting material Si_3N_4 and tungsten, respectively. ν_1 and ν_2 and are the mass absorption coefficient of Si_3N_4 and tungsten, respectively. h_1 is the thickness of Si_3N_4 and h_2 is the thickness of the thin layer of tungsten.

With sub-35nm critical dimension, large area parallel exposure capability, elimination of need for vacuum, and potentially low cost, SPEL could be used to realize top-down fabrication nanostructure arrays. As an example, we successfully used SPEL to fabricate vertical silicon nanowire arrays (Fig. 4) over a 4-inch wafer, with both controllable nanowire diameter and pitch density. Nanowire solar cells have been predicted and demonstrated to have the capability to have high light absorption efficiency[3]. These nanowire arrays, fabricated by SPEL, are possible to be used for high efficiency solar cells and other energy devices application, which need large area.

References:

1. C. Vieu *et al*., "Electron beam lithography: resolution limits and applications", *Applied Surface Science*, **164**, 111-117 (2000).
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3. B. M. Kayes, H. A. Atwater, N. S. Lewis, "Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells", *J. Appl. Phys.* 97, 114302 (2005).

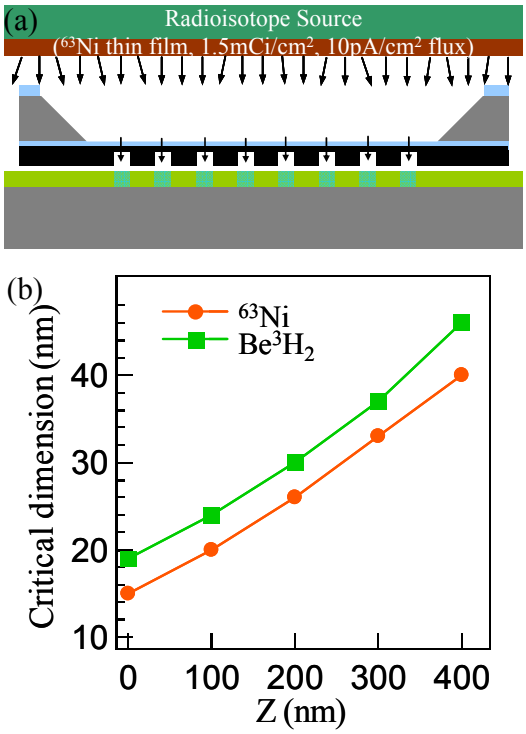

Figure 1: (a) Schematic of SPEL experimental set up. Electrons emitted from a ^{63}Ni (or tritium Be^3H_2) source are captured by the ebeam resist after illuminating from the stencil mask. (b) Monte Carlo simulation for curves *critical dimension (CD) vs mask resist gap Z.*

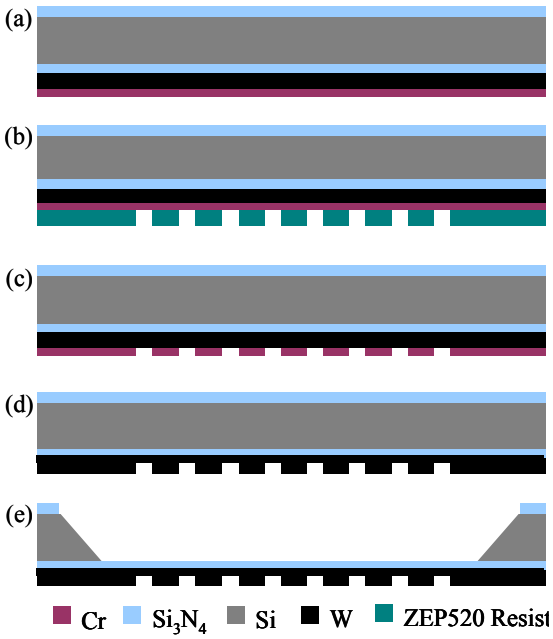

Figure 2. SPEL mask fabrication process. (a) Low stress LPCVD nitride (1500nm) deposition on double polished Si (100) wafer, followed by 150nm of W sputtering and 20nm of Cr evaporation on the front side. (b) E-beam patterning, using ZEP520 resist. (c) Cr RIE etching, using ZEP520 as the etching mask. (d) W RIE (CF_4/SF_6) etching, using Cr as etching mask. (e) Back side nitride window patterning by optical lithography, nitride RIE etching, followed by KOH (80°C) Si etching to etch through the Si wafer.

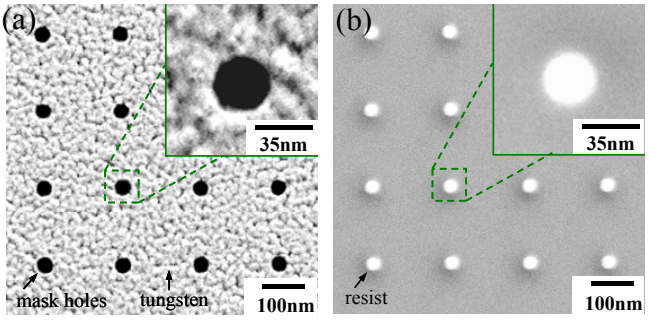

Figure 3: (a) SEM images of the tungsten mask, with 35nm holes arrays. (b) SEM images of the corresponding NEB31A resist pattern (~60nm in thickness), created by the mask in (a), using SPEL system with ^{63}Ni thin film source.

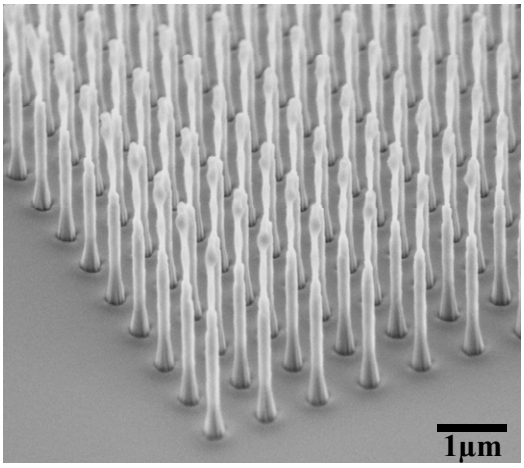

Figure 4：SEM image (45°C side view) of the vertical Si nanowire arrays, patterned by SPEL, followed by Si RIE etching with Cr and SiO_2 as the etching mask.