Sub-10 nm Nanochannel Fabrications by Self-Sealing and Self-Limiting Atomic Layer Deposition

Sung-Wook Nam[1], Min-Hyun Lee[1], Seung-Hyun Lee[1], Do-Joong Lee[1], Stephen M. Rossnagel[2] and Ki-Bum Kim[1]

[1]*Materials Science and Engineering, Seoul National University, Seoul 151-742, Korea*
[2]*IBM. T. J. Watson Research Center, Yorktown Heights, New York 10598*

The electrical manipulation of ions and bio-molecules is a promising direction for bio-health applications of electrofluidics. In nanopore or nanochannel fluidic devices, surface charges of the channel wall cause a screening effect by leading the counter-charged ions to be accumulated near the channel wall. These ions eventually serve as majority carriers, which allows for a unipolar transport behavior in ionic current. Electric manipulation of ionic current is possible by gate-electric bias through ionic field effect transistor (IFET) device.[1] In order to utilize surface charges in electrofluidic system, reliable fabrication of nanopores or nanochannels is essential with molecular-level feature size, namely, sub-10 nm.

Here, we report a novel fabrication method of nanochannel structures through atomic layer deposition (ALD) in which highly conformal films can be obtained. Our fabrication starts with line trench structure defined by conventional lithography process. In trench structure, isotropic wet etching leads undercut geometry we call as "pipe structure". Along the pipe structure, ALD film makes it sealed by dielectric film, leaving the void at the center of pipe. In particular, the size of void is self-limited by the undercut dimension due to the highly conformal film deposition process. So-called self-sealing and self-limiting ALD (SS-ALD) provides us a tremendous benefit that leads sub-lithographic dimension in the nanochannel size, as shown in Figure 1. As a proof-of-concept, we used a-Si/SiO_2 films available for highly selective wet etching process in dilute HF solution. The pipe structures were generated, and then the void structures were constructed by the SS-ALD as Figure 2. By changing the wet etching time, we could control the void dimension beyond the lithographic limitation, namely sub-10 nm, as Figure 3. In advance, for the demonstration of IFET through SS-ALD process, we used Ru/Al_2O_3 bi-layer ALD films. Ru metal layer surrounds the nanochannel, so the gate electric bias can control the ionic current through nanochannel as described in Figure 4. The all-around-gating IFET structure was demonstrated by a sequential film deposition of Ru and Al_2O_3. The void structure with ~20 nm dimension was surrounded by Al_2O_3 and Ru which have roles of gate dielectric and gate metal, respectively, as shown in Figure 5. Most of all, the final size of the void was only determined by the wet etching time regardless of the initial trench dimension and the ALD film thickness as shown in Figure 6. This self-limiting process may provide a wide process window in the fabrication of sub-10 nm nanochannel structures. Finally, on the basis of SS-ALD process, we demonstrated a full integration scheme of nanochannel IFET as shown in Figure 7. After generating pipe structures, we patterned Ru electrode for gate-bias probing. Then, SS-ALD of dielectric film led the nanochannels embedded in the substrate. Channel opening process was carried out by patterning reservoirs at both ends of nanochannels. Polydimethylsiloxane (PDMS) chamber was assembled with nanochannel IFET chip in order to guide electrolyte liquid into the core IFET region.

(1) S. W. Nam, M. J. Rooks, K. B. Kim, and S. M. Rossnagel, *Nano Lett.* 9, 2044 (2009)

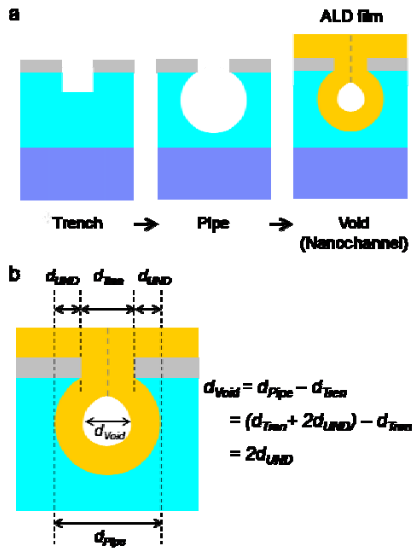


Figure 1 (a) Self-sealing and self-limiting atomic layer deposition (SS-ALD) for nanochannel fabrication. (b) Size determination principle, namely self-limiting process: The size of void is only determined by the undercut dimension.

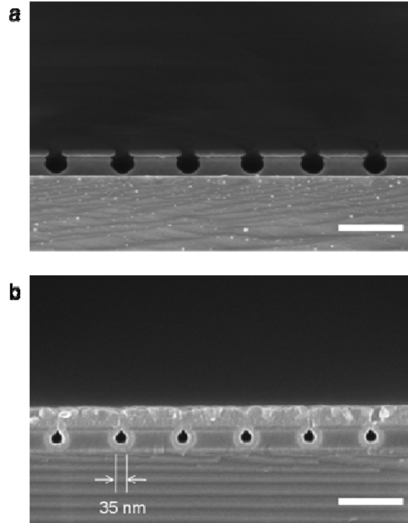


Figure 2 (a) SEM image of pipe structure fabricated by isotropic wet-etching process. (b) Nanochannels by SS-ALD. (All scale bars 200 nm)

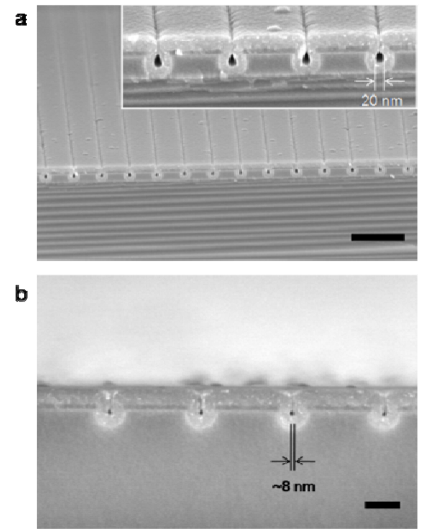


Figure 3. Size controllability of SS-ALD: Sub-lithographic dimensions such as (a) ~20 nm and (b) ~8 nm are demonstrated. (Scale bars: 500 nm (a), 100 nm (b))

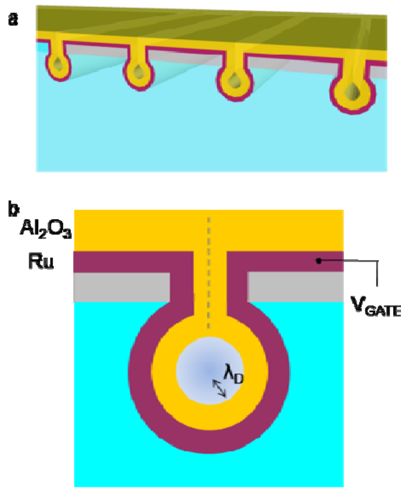


Figure 4. (a) Core/shell (dielectric/metal) nanochannels for all-around-gating ionic field effect transistors (IFET). (b) The ionic screening region determined by Debye screening length is expected to be controlled by gate bias (V_{GATE}).

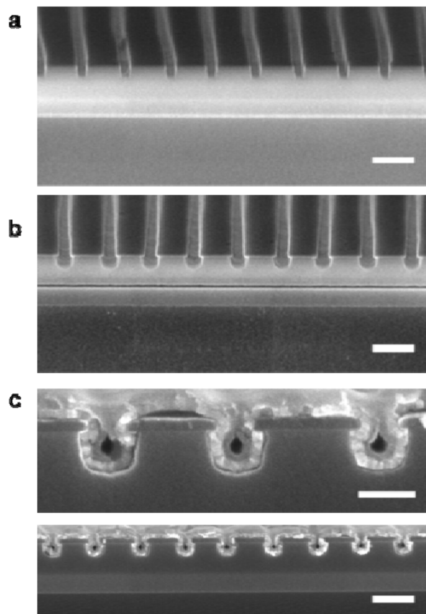


Figure 5. Core/shell nanochannel fabrication: (a) Trench (b) Pipe and (c) Nanochannel. (Scale bars: 250 nm (a,b,c bottom), 100 nm (c top))

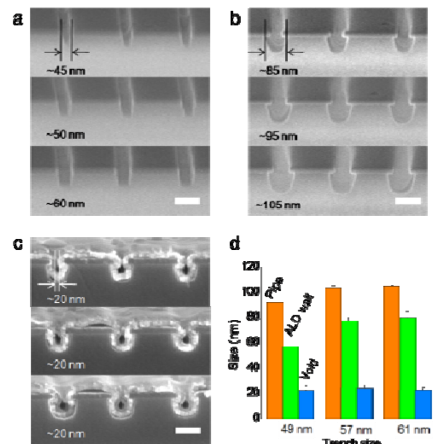
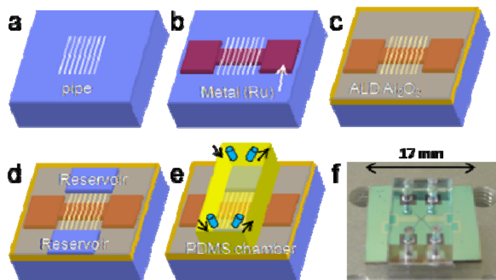


Figure 6. Evaluation of self-limiting behavior: The wet etching time was same for three samples. Although the dimensions of (a) trench and (b) pipe are different among three samples, (c) the void structures have the same dimension such as ~20 nm. (d) The void dimension is only determined by the wet etching time. (All scale bars: 100 nm)



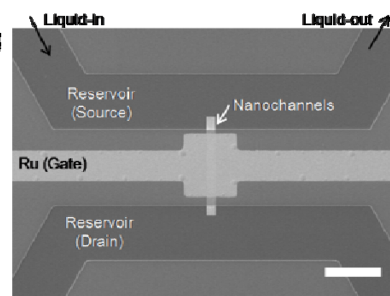


Figure 7. Full integration scheme for all-around-gating IFET chip using SS-ALD (a) Pipe structures (b) Patterning of metal ALD metal film (c) SS-ALD of dielectric film (d) Reservoir structures (e) PDMS assembly (f) Optical microscope image of chip (g) SEM image of the core IFET region. (Scale bar: 100 um)