Mask Aligner Lithography Simulation

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Keywords: simulation, mask aligner, photoresists, optical lithography, modeling, Layout Lab

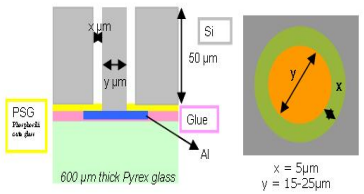
Optical lithography is a key process step for making semiconductor devices. Proximity and contact printing is frequently utilized at universities, research centers, and also small to medium enterprises, since it offers a less complex and more cost efficient solution over projection printing. There, the wafer with a deposited photoresist layer is brought in a close proximity of several microns to the 1:1 mask, creating the lithographic image inside the photoresist by shadow projection of the mask pattern.

The proximity and contact printing processes are not trivial even if the typical feature size is in the range of some microns. The thick resist with high topography increases the complexity of the process and requires the optimization of different parameters including mask design, photoresist types, coating parameters, illumination source type/spectrum, proximity gap between wafer and mask, post exposure bake and resist development. These process parameters are typically optimized experimentally for each new process. Usually several experiments have to be carried out to find the optimum process settings, which has a negative impact on i) getting results quickly, ii) production line throughput and iii) costs. As an alternative to experiments, a simulation software like LayoutLab [1,2] can be used to reduce the number of required experiments and to verify process parameters. The software was designed to model optical lithography using mask aligners, an area typically not covered by lithography simulators. LayoutLab is capable to model the entire lithographic process flow including exposure, post-exposure bake and resist development.

This paper shows the use of lithography simulation to aid in understanding photoresist behavior in some example applications. The first example shows a Through Silicon Via (TSV) process with a ring pattern (Figure 1a and 1b). The circular trench has typically an inner diameter of 25µm and a depth of 5µm. A significant issue here is the resist attack at the centre of the ring due to the specific light intensity pattern formed by diffraction (Figure 2: experimental result, Figure 3: simulation example). The small trench in the resist at the centre, depending on its extent, can have a detrimental impact on the subsequent dry etching step. The paper explains how simulation can help to understand and minimize the effect.

The second example is concerned with proximity gap validation, a general issue with mask aligners. During exposure, a gap is maintained between mask and wafer to avoid mask damage or contamination. On one hand, the gap needs to be large enough to avoid intimate contact between mask and wafer. On the other hand, it should be kept small to ensure the highest possible resolution. The gap may vary across the wafer because of non-flatness of mask/wafer, or contamination particles. Using specific test structures and comparing experimental and simulated results it is it is possible to determine the difference between the set and the actual gap, and the gap variation across the wafer.

[1] M. Cucinelli et al., Mask Aligner Lithography: Pushing the Limits, poster presentation at MNE 2006
[2] A. Malzer et al., Simulation software enables DFM for MEMS, Solid State Technology, December 2007



a b

Figure 1, a: cross-view and b: top-view of a ring-shaped TSV on bonded Pyrex wafer

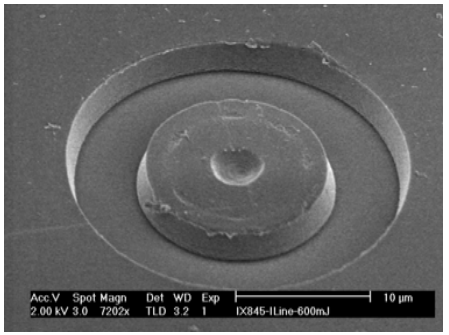


Figure 2. Scanning Electron Micrograph of a ring pattern showing the resist attack at the centre

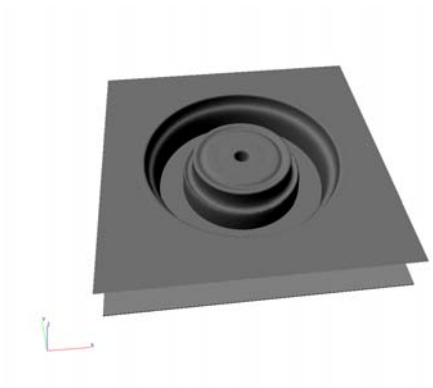


Figure 3: 3D view of the resist profile after full simulation, exposure and development. The gap was fixed at 10µm and a dose of 75mJ/cm² was used.