CMOS density scaling in non-planar multi-gate silicon on insulator devices

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Developing the patterning techniques to achieve denser levels of CMOS integration is a critical component of each new technology node. However, the era of CMOS density scaling enabled primarily by the reduction of critical dimensions and feature pitch has long since come to an end. For example, the advent of high-k/metal gate technology combined with advanced junction engineering provided the critical breakthroughs required to achieve the performance targets of the 32 nm node technology[1]. Extensions of these elements should result in continued scaling without changing the fundamental design of the transistor used in the 22 nm technology[2].

While it is possible that conventional planar Si CMOS will continue to be used in the 14 nm node, the requirements for the gate dielectric and junction depth needed to maintain control of short channel effects may prove to be unobtainable. Consequently, an additional method for improving the electrostatics of the device is required. This realization has driven a steady increase in research on non-planar multi-gate CMOS devices over the past 5 years. Raising the Si channel out of the plane of the substrate creates the opportunity to form the gate electrode around multiple sides of the channel. This geometry results in a superior situation from an electrostatics standpoint compared to a planar device where the gate electrode is present only on the top surface of the channel[3].

In this talk, we will discuss the challenges of fabricating three non-planar multi-gate devices from Si on insulator (SOI) substrates: (1) the FinFET[4], where the gate controls two sides of a thin Si mesa or fin (2) the Trigate[5] where the gate controls three sides of a Si fin and (3) a gate-all-around nanowire transistor[6] where the gate electrode surrounds all sides of a suspended Si channel. We will present experimental results from advanced prototypes of these devices fabricated at dimensions relevant to 14 and 10 nm node technology. An emphasis will be give to the unique patterning and process integration requirements for building these devices at feature pitches below 60 nm. These results offer insight into what may lie ahead for Si CMOS scaling and how it will impact the demands placed on patterning.

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