# Progress in Jet and Flash Imprint Defectivity Reduction Towards Semiconductor Manufacturing Requirements

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Nanoimprint lithography continues to make progress towards meeting high volume manufacturing requirements for semiconductor devices. Demonstrations have shown that it meets, or is close to meeting, 22nm node requirements for resolution, critical dimension uniformity, line width roughness, and template pattern placement. Even overlay, once considered a major roadblock, has improved to within a factor of two of the requirement for 22nm flash specified in the International Technology Roadmap for Semiconductors. However, defectivity is still identified as a leading technical challenge to the implementation of nanoimprint lithography in high volume manufacturing. The lack of confidence in nanoimprint's ability to meet defect requirements originates in part from the industry's past experiences with 1X lithography and the shortage in end-user generated defect data. SEMATECH has therefore initiated a defect assessment aimed at addressing these concerns. The goal is to determine if nanoimprint is capable of meeting semiconductor industry defect requirements.

Several cycles of learning have been completed in SEMATECH's defect assessment. Proof of concept for process random defectivity of $< 0.1$ def/cm$^2$ has been demonstrated, as shown in Figure 1, using a high quality, large field, 120nm half-pitch template. Template and particle defects were removed during the analysis to demonstrate process capability under ideal conditions. Template defectivity has also improved. Figure 2 shows defects representative of a pre-production grade template at an 80nm pitch.

Defect types will be explained, and requirements for a low defect nanoimprint process with be discussed. In addition, plans for continued cycles of defectivity learning on feature sizes down to 22nm, and an overall assessment of Jet and Flash Imprint Lithography defectivity will be shared.

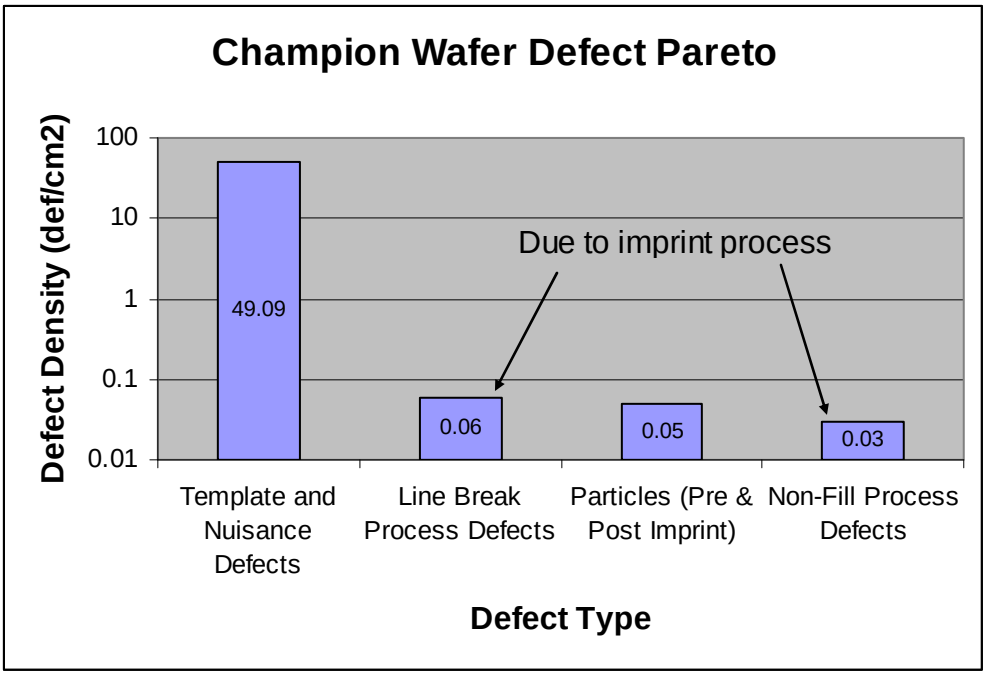


*Figure 1: Champion wafer defect pareto (log scale):* <0.1def/cm$^2$ due to imprint process. Wafer printed using a 26mm x 30.65mm field containing 120nm half-pitch line/space features. Process defect density after removing template and particle defects.

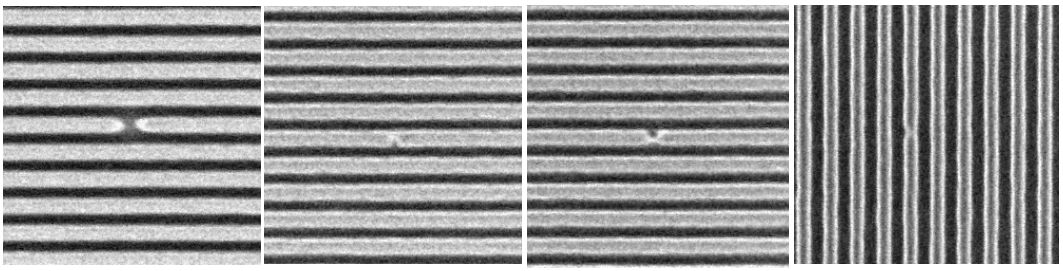

*Figure 2: Examples of template defects from a pre-production grade template:* Demonstration of the improvement in template defect type and size as observed using a full field, vector-shaped beam written template at 80nm pitch (44nm lines and 36nm spaces). Template defects as captured at the wafer level.