Arrays of 25 × 25 nm^2 Cross-Point Resistive Switching Devices Fabricated with Nanoimprint Lithography

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Transition metal oxide based resistive switching devices (memristors) are promising candidates for the next generation non-volatile random access memory (NV-RAM) [1, 2]. Due to its simplicity and scalability in structure, cross-point architecture has been widely used for these devices. Nanoimprint lithography (NIL) [3] has proved to be the cost-effective technique for fabricating working TiO_2-based devices with junction area of 50×50 nm^2 [4].

Here we present arrays of TiO_2-based cross point resistive switching devices with junction area of 25×25 nm^2 using NIL. To fabricate the imprint mold, we started with a master mold (100 nm thick thermal SiO_2 on Si) that has arrays of 50 nm wide nanowires and microscale fanouts and contact pads patterned by electron beam lithography (EBL) and photolithography. Diluted HF (1:50) was then used to shrink the feature size and the lateral etching rate of SiO_2 is about 1.1 Å/s (Figure 1). With careful control of the etching time, and constant stirring of the solution (~1Hz magnetic spin bar), the line width of the SiO_2 mold was shrunk to 25 nm (Figure 2). The features were then duplicated to a quartz (QZ) substrate using NIL and reactive ion etching (RIE).

In device fabrication, we used NIL for both the bottom and top electrodes. First, double layer resists consisting of an underlayer that dissolves in acetone and a UV-curable top layer that cross-links upon the UV radiation were spin coated onto a SiO_2/Si substrate. UV-NIL using the QZ mold was then carried out to pattern the device structures into the UV-curable layer. The residual cross-linked UV resist and the underlayer were etched by RIE using fluorine and oxygen based etching chemistry, respectively. After depositing 4 nm Ti and 12 nm Pt in an electron gun evaporator and a lift off process in acetone, a 29 nm thick TiO_2 film was sputter coated onto the substrate at a temperature of about 270°C in a direct current (DC) sputtering system. Lastly, the top electrode (16 nm thick Pt) was fabricated on the TiO_2 switching layer using NIL, RIE, metal deposition and liftoff. Fig. 3 shows scanning electron microscope (SEM) images of the device arrays with junction area about 25×25 nm^2.

The current method provides a simple approach to make cross point devices with small junction areas. The electrical characterization of the small-area devices will also be reported.

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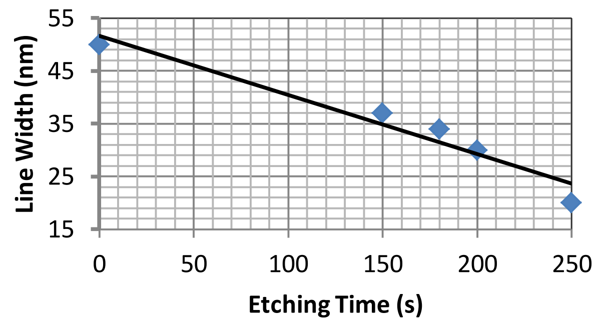

Figure 1. The line width of an originally 50 nm wide SiO_2 nanowire mold as a function of etching time in 1:50 diluted HF solution. The solution was constantly stirred using a magnetic spin bar at 1 Hz.

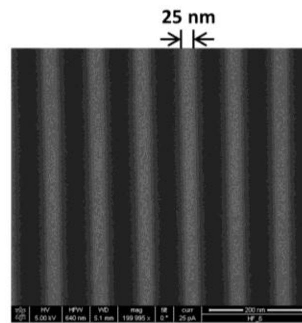

Figure 2. SiO_2/Si mold of 25 nm line width that was shrunk from the original 50 nm ones using diluted HF etching.

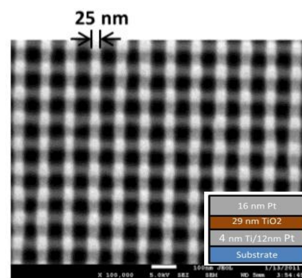

Figure 3. An array of cross-point devices with 25×25 nm^2 junction areas. The cross sectional device geometry is schematically shown in the inset (not to scale).