Impact of EUV lithography line edge roughness on 16 nm memory generation

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Resist roughness is one of the main effects of process uncertainties in Extreme UV lithography. All of the lithographic elements, such as the source, the mask, the optical system, the resist and the metrology, contribute to the Line Edge Roughness due to the natural stochastic behavior of UV photons, photogenerated electrons, acids and polymer deprotection[1]. As a result, Line Edge Roughness in Extreme UV lithography is still a challenge to be tackled for 22 and 16 nm electrical devices[2].

In this paper, the impact of post-litho smoothing processes[3], such as ion-beam sputtering and plasma etch treatment on state-of-the-art 32 nm half-pitch Extreme UV resists, is reported. Top- down and cross section Scanning Electron Microscopy (Figure 1a) were used to evaluate the low and high frequency components of Line Edge Roughness by means of Power Spectral Density analysis[4] (Fig. 1b). To compute surface tension calculation, line edge profiles were first rebuilt (Figure 1c), and then injected in a Monte-Carlo variability aware simulator for electrical failure evaluation of a 16 nm multi-level NAND Flash memory array[5] (Figure 1d).

Electrical simulations driven by real roughness profiles were executed in order to quantify the impact of Line Edge Roughness on reliability of 16 nm ½ pitch devices. Through the variability aware model, it was found that low frequency Line Edge Roughness generated in the optical system range, impacts the memory performance, with a failure factor 5 times higher compared to the same electrical model without considering any variation caused by roughness (Figure 2).

Finally, by combining both resist roughness and electrical assessment, it was possible to quantify the contribution of post-litho smoothing processes on the electrical performance of memory devices.

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[5] P. Poliakov, et all, "Cross-cell interference variability aware model of fully planar NAND Flash memory including line edge roughness", *Microelectron Reliab.* (2010)

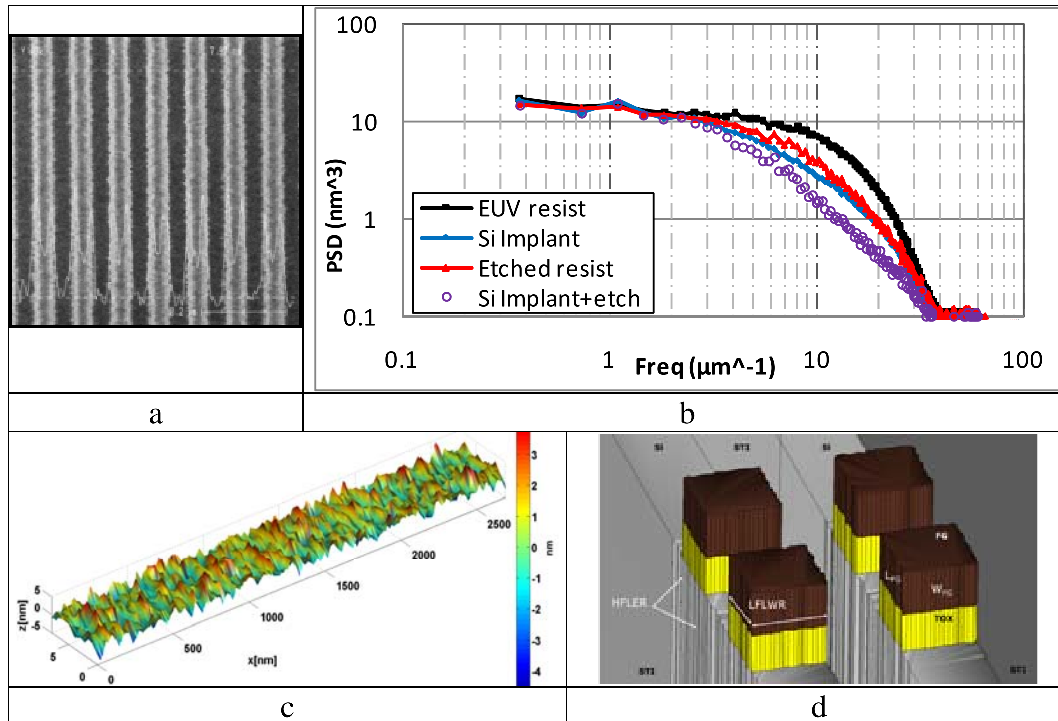

Figure 1: experimental roughness in electrical simulator: in the picture, roughness measure, characterization, and evaluation are shown. a) top-down Scanning Electron Microscopy picture of 32 nm ½ pitch EUV resist, b) Power Spectral Density extraction from line edges, c) edge roughness reconstruction d) 2x2 NAND Flash cell array test vehicle with Line Edge Roughness injection.

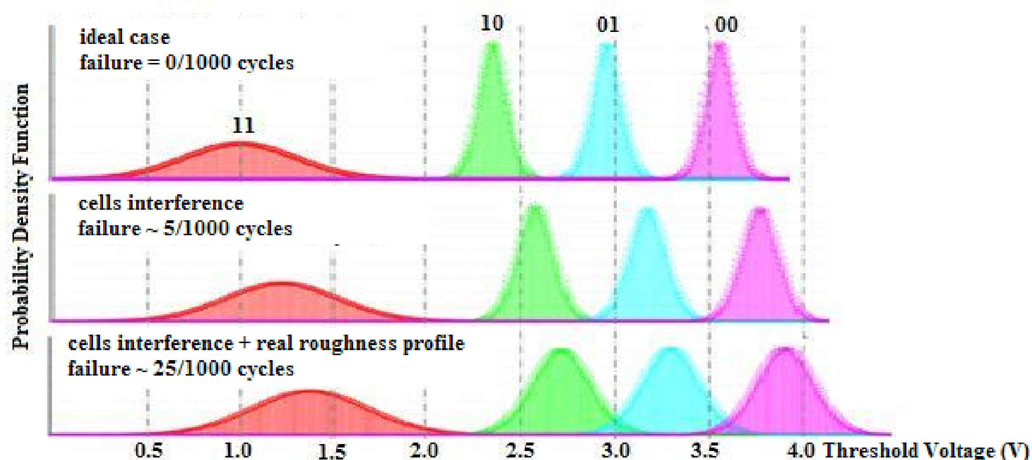

Figure 2: Probability Density Function for 16 nm ½ pitch multi-level NAND Flash memory: 3 graphs are shown: Threshold Voltage probability distribution for a memory array considering 1) ideal case 2) cell-to-cell interference 3) cell-to-cell interference plus real line roughness profile. In the last case, substantial Threshold Voltage distributions shift and broadening were found, causing cell content read failures.