Challenges for Patterning Process Simulation Models applied to Large Scale

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Full-chip patterning simulation has been utilized in semiconductor manufacturing for more than ten years, and has been a key enabler for multiple technology generations, from 130 nm to the emerging 14 nm node. This span has featured two wavelength changes, a progression of optical NA increases (and a subsequent decrease), and a variety of patterning processes and chemistries. Full-chip patterning simulation has utilized quasi-rigorous optical models and semi-empirical resist and etches process models. There has been steady improvement in the predictive power and runtime performance of the semi-empirical patterning models used in full chip simulation tools, and this paper will review this progress as well as the factors which ultimately limit the predictability of such models. In addition, this paper will outline the new process simulation challenges which emerge as the industry approaches sub-0.25 k1 patterning. These challenges lie principally in improving the accuracy of representing patterning processes, including 3D effects, for an expanding set of processes and failure modes, while maintaining or improving full chip data preparation cycle times.