Vertical Transistors with High Alignment Tolerance

L. W. Tutt, S. F. Nelson
Eastman Kodak Company, 1999 Lake Avenue, Rochester, NY 14650-2142
lee.tutt@kodak.com

Patterning and alignment of the transistors on a flexible support continues to be a challenge for submicron channel lengths. In this paper we present a vertical transistor architecture that has both high alignment tolerance as well as submicron channel lengths and is further compatible with flexible supports. This condition is accomplished by constructing vertical devices that are conformally coated and combined with a beam (line-of-sight) deposition process such as sputtering or evaporation.

Spatial Atomic Layer Deposition (S-ALD) is an atomic layer deposition process that is compatible with roll-to-roll processes. S-ALD has been shown to give high-quality ZnO FET transistors[1]. Both the semiconductor and the gate dielectric were deposited by this technique. As an ALD process, it yields very controlled thicknesses over highly variable topography. This control, coupled with conformal coating, is ideal for a vertical transistor process.

Using a reentrant profile over a gate, we show that S-ALD gives uniform coatings that maintain the reentrant profile. Deposition of the drain-source electrodes by a beam deposition process automatically yields a transistor. A cross-sectional SEM of one transistor architecture that employs this approach is shown in Figure 1. In this figure, a dielectric of aluminum oxide overhangs the gate metal electrode to give the reentrant profile. The sample was then conformally coated with the insulator and semiconductor. Evaporative deposition of aluminum yielded the drain and source.

SEM, TEM, and electrical characterizations are presented, which show expected asymmetries in the drain-source as well as the impact of ungated regions. Improvements in the design architecture are shown to minimize the ungated channel regions while they maintain alignment tolerance and electrical properties. In the best design, the transistor's drain current ranges from about 10^{-11} amps at a gate of -2 volts to almost a milliamp at a gate of 10 volts, for a drain voltage of 1.2 volts.

[1] D. H. Levy, S. F. Nelson, and D. Freeman, J. Disp. Tech. **5,** 484 (2009)

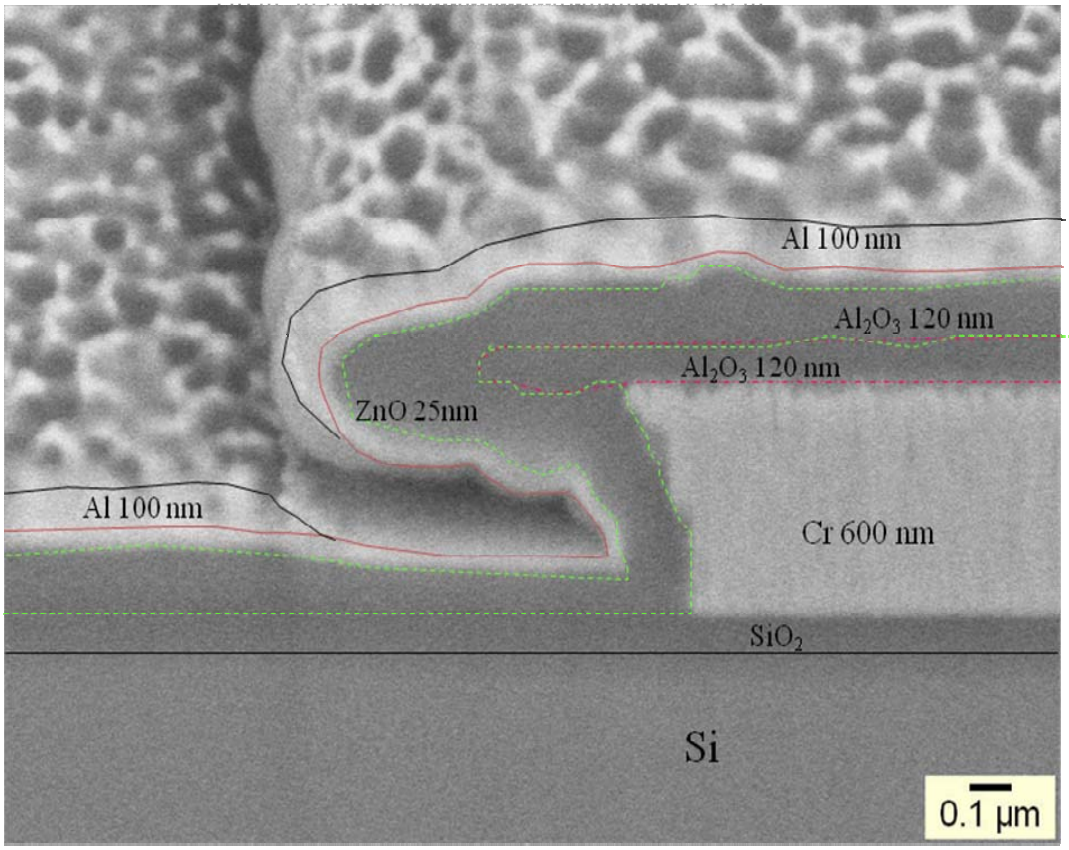

Figure 1: Cross sectional view of a vertical transistor: The SEM picture shows the reentrant profile as well as the excellent conformal coating properties of the S-ALD process. Pitting of the aluminum electrodes was incurred during the focused ion beam (FIB) cross-sectioning.